Adaptive Inter-chip Interference Cancellation of Multirate Scrambled CDMA Downlink

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Abstract

We propose an adaptive two-stage receiver for a scrambled multirate DS-CDMA downlink. The first stage consists of adaptive FIR equalization generating tentative hard decisions, while the second stage involves adaptive inter-chip interference (ICI) cancellation. Here we detail the adaptive ICI stage, which is based on a low-complexity decision-directed LMS channel identification algorithm; the first stage has been described in a previous publication [1].

1 Introduction

In third generation mobile DS-CDMA systems, downlink multirate symbol streams are multiplexed using orthogonal short codes and then scrambled by a cell-specific long code prior to synchronous transmission. The multipath propagation channel creates inter-chip interference (ICI) in the received signal, which destroys the orthogonality among user codes. While linear FIR equalization can reduce multi-access interference (MAI) by re-orthogonalizing the chip-rate signal prior to the despreading operation (e.g., [1]), non-linear processing offers potentially better performance. In [2], tentative chip decisions are used in decision feedback equalization (DFE), but only single-user ICI cancellation is accomplished and the structure is not amenable to adaptation. In [3], a chip-level equalizer output is soft-decoded to obtain estimates of all active symbol streams. These estimates are fed-forward, respread, and used as feedback information for re-processing the received signal via chip-level DFE, cancelling post-cursor ICI.

2 Inter-Chip Interference Cancellation

In this paper we propose an ICI-cancellation stage capable of eliminating both pre- *and* post-cursor ICI. Several branches—each corresponding to a different "cursor"—are maximal-ratio combined (MRC) to leverage multipath diversity, as shown in Fig. 1(a). N_{max} is the spreading factor of the lowest-rate user, ν is the system delay through the first stage, $\boldsymbol{r}_{i-N_{max}-\nu}$ is the delayed-received signal, $\hat{t}_{i-N_{max}-\nu}$ is the detected multiuser chip-rate signal, and $\{\hat{\boldsymbol{h}}_i\}$ is the 1/2-chip spaced channel estimate. (See [4] for a more detailed exposition.) For sparse channels, MRC combines only the largest ICI-cancellation branches. Adaptive LMS channel estimation uses $\hat{t}_{i-N_{max}-\nu}$ as training:

$$\boldsymbol{e}(i) = \hat{\boldsymbol{h}}^T(i)\hat{\boldsymbol{t}}(i-N_{max}-\nu) - \boldsymbol{r}_{i-N_{max}-\nu} \quad (1)$$

$$\hat{\boldsymbol{h}}(i+1) = \hat{\boldsymbol{h}}(i) - \mu \boldsymbol{e}^T(i) \otimes \hat{\boldsymbol{t}}^*(i-N_{max}-\nu). \quad (2)$$

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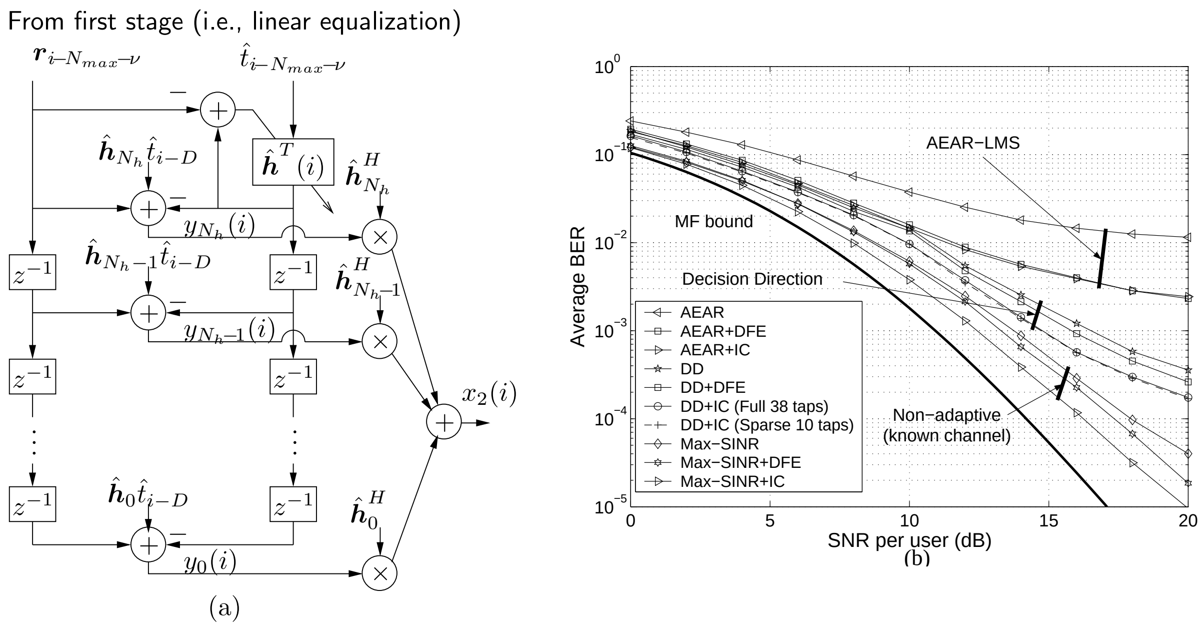

Figure 1: (a): Block diagram of adaptive ICI-canceller. (b): Uncoded BER performance of adaptive and optimal (non-adaptive) algorithms for a half-loaded multirate CDMA downlink with mobile speed of 60 km/hr, 4-chip Rayleigh-fading exponential channel power profile, and 0.22 excess bandwidth. First-stage equalizers span 25 chips (50 taps) and performance is averaged across users. A more detailed description of the simulation can be found in [4].

where $\otimes$ denotes the Kronecker product. Final bit decisions are made from $x_2(i)$.

3 Simulations and Conclusions

Three sets of BER curves are shown in Fig. 1(b) along with the matched filter (MF) bound. Each set shows the result of first-stage linear processing (either AEAR, DD, or Max-SINR) with the possible addition of a second nonlinear processing stage (either DFE or IC). AEAR and DD refer to linear FIR equalizers adapted via pilot-training and decision-direction, respectively, as described in [1], while Max-SINR refers to the SINR-optimal linear FIR equalizer, requiring perfect time-varying channel knowledge. We attribute the superiority of the adaptive ICI canceller "IC," relative to the adaptive DFE (e.g., [3]), to its simultaneous pre- and post-cursor ICI cancellation ability. Furthermore, ICI cancellation with sparse MRC (10 largest taps) performs on par with full MRC (38 taps). Both IC and DD outperform linear processing alone.

References

[1] P. Schniter and A. Margetts, "Adaptive chip-rate equalization of downlink multirate wideband CDMA," *Proc. Asilomar Conf. on Signals, Systems and Computers*, Nov. 2002.

[2] J. Yang and Y. G. Li, "A decision-feedback equalizer with tentative chip feedback for the downlink of wideband CDMA," *Proc. IEEE Intern. Conf. on Communication*, vol. 1, pp. 119–123, Apr. 2002.

[3] J. F. Roessler, W. H. G. Lutz H.-J. Lampe, and J. B. Huber, "Decision-feedback equalization for CDMA downlink," *Proc. IEEE Vehicular Technology Conference*, vol. 2, pp. 816–820, May 2002.

[4] A. Margetts and P. Schniter, "Chip-rate adaptive DFE of scrambled downlink CDMA," *Proc. Asilomar Conf. on Signals, Systems and Computers*, Nov. 2003.