Automatic Algorithm for the Direct Design of Asymmetric Doherty Power Amplifiers

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***Abstract* — This paper presents a novel method for the direct design of asymmetric Doherty power amplifiers (PAs). Single-transistor class F and C simulations for the main and auxiliary amplifiers respectively are first performed at both peak and backoff powers using the intrinsic IV characteristics. A 1-D transcendental equation is then solved to create the Doherty prototype at the intrinsic reference planes. The Doherty output combiner at the package reference planes is finally obtained using non-linear embedding. This direct design method is implemented in an automatic algorithm, which produces a functional DPA prototype in typically 95 seconds. A dual-input DPA operating at 2 GHz is fabricated using two identical 15 W packaged GaN transistors. A drain efficiency of 69% at peak power (42.9dBm) and 63 % at 9 dB backoff (33.9 dBm) are observed using continuous wave (CW) measurements. The measured gain is above 14 dB. The PA dynamic response is verified with a 10 MHz LTE signal with a 9.9 dB peak to average power ratio (PAPR). 51.3% average efficiency is achieved after linearization with -45.5 dBc adjacent channel leakage ratio (ACLR).**

***Index Terms* — Doherty Power amplifiers, embedding.**

I. Introduction

Doherty PAs are currently amongst the most widely used PA architectures in modern wireless communications, due to their simple implementation and improved average efficiency for modulated signals exhibiting large PAPR. Conventional Doherty PAs [1] rely on a quarter-wave transformer connecting the main to the common load, to implement a mutual load modulation between the main and auxiliary PAs. For realistic transistors used at microwave frequencies, the parasitic effects at the package reference planes are of crucial importance. Typically, loadpull measurements or simulations are used to search for the optimal multiple harmonic impedances. Impedance transformers and offset lines are then added to convert the complex loads to resistive loads, or the Doherty combiner can be directly synthesized from the complex loads with a non-90° input phase offset [2].

An alternative design-approach that utilizes the non-linear embedding device model has been reported in [3] [4], [5] and [6]. In this approach a Doherty PA prototype is first implemented at the current-source reference planes using the devices' intrinsic IV characteristics before projecting the voltages and currents from the intrinsic to the package reference planes using nonlinear embedding. This approach eliminates the need for multi-harmonic loadpull.

In this work, an algorithm for automatically designing intrinsic Doherty PAs is presented. This algorithm relies on exact design equations that account for the finite impedance of the auxiliary PA at backoff.

Section II of this paper discusses the details of the Doherty design theory and algorithm. Multiple Doherty PA prototypes are automatically realized and compared. Section III presents the measurement data of a fabricated Doherty PA based on the algorithm introduced in this paper. Section IV summarizes the new contributions made.

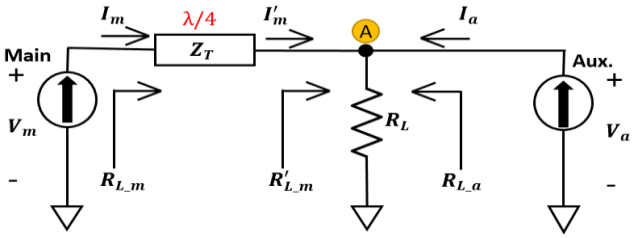

Fig. 1 Conceptual Doherty PA at the current source reference planes.

II. Automatic Design of a Doherty Power Amplifier

The ideal Doherty PA targeted at the current-source reference planes is shown in Fig. 1. The current sources represent the IV-characteristics of the main and auxiliary transistors. The impedance inverter with characteristic impedance Z_T is placed between the main transistor and the common load R_L connected at the junction node A. The intrinsic RF drain voltage seen by the main transistor is defined as:

$$V_m = I_m \cdot R_{L\_m} \tag{1}$$

where R_{L_m} varies according to the load modulation at the junction node A. Applying the ABCD matrix of the impedance inverter with characteristic impedance Z_T, the RF drain voltage in (1) is further expressed by:

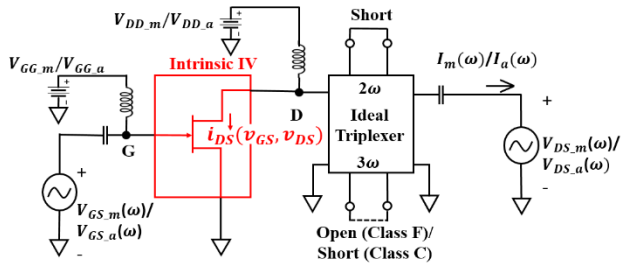

Fig. 2 Single-transistor simulation of a main or an auxiliary amplifier at the current source reference planes.

$$V_m = -jZ_T I_a + I_m \frac{Z_T^2}{R_L} \tag{2}$$

Assuming that the fundamental currents and voltages seen by the main and auxiliary devices at both backoff and peak powers are denoted by $\{V_{mp}, V_{mb}\}$, $\{I_{mp}, I_{mb}\}$, $\{V_{ap}, V_{ab}\}$ and $\{I_{ap}, I_{ab}\}$, respectively, the impedance seen by the auxiliary device at peak power level R_{L_a} can be verified to be given by:

$$R_{L\_a} = \frac{|V_{ap}|}{|I_{ap}|} = \frac{|I_{mp}|}{|I_{ap}|} \cdot \frac{|V_{mb}|\cdot|I_{mp}| - |V_{mp}|\cdot|I_{mb}|}{|I_{mb}|\cdot|I_{ap}| - |I_{mp}|\cdot|I_{ab}|} \tag{3}$$

However, for an optimal efficiency and output power, the impedance R_{L_a} seen by the auxiliary device should ideally be the optimal impedance R_{opt_a}. Thus a necessary condition to achieve a high-efficiency Doherty topology is to make:

$$R_{L\_a} = R_{opt\_a}. \tag{4}$$

In this design, the voltages: $V_{mp} = V_{mb} = V_{DD\_m} = 15$ V, $V_{ap} = V_{DD\_a} = 30$ V and the current $I_{ap} = 1$ A are used. To solve the transcendental equation (4), the gate biases and the outputs I_{mp}, I_{mb}, V_{ab} and I_{ab} currents are calculated in four successive 1D-swept harmonic-balance simulations (Steps 1 to 4) to be described next.

The characteristic impedance of the inverter Z_T and the common load R_L shown in Fig. 1 are then calculated using

$$Z_T = \frac{|V_{mb\_opt}|\cdot|I_{mp\_opt}| - |V_{mp\_opt}|\cdot|I_{mb\_opt}|}{|I_{mb\_opt}|\cdot|I_{ap\_opt}| - |I_{mp\_opt}|\cdot|I_{ab\_opt}|}. \tag{5}$$

$$R_L = \frac{|I_{mp\_opt}|\cdot Z_T^2}{(|V_{m\_opt}| + |I_{ap\_opt}|\cdot Z_T)}. \tag{6}$$

In (5) and (6) the optimum values obtained from the solution of (4) are noted with the subscript *opt*. Notice that the optimum gate voltage drives at both peak and backoff are also obtained for the main and auxiliary transistors, respectively. The algorithm steps are as follows:

Step 1. Simulate the auxiliary PA at peak power: Set the drain bias voltage V_{DD_a} of the auxiliary PA and the fundamental RF drain voltage swing $|V_{ap}|$ using a voltage source as shown in Fig. 2. Sweep the input gate voltage $|V_{gs\_ap}|$ at peak power to obtain the targeted fundamental current $|I_{ap}|$. The gate bias is calculated using $V_{GG\_a} = V_T - |V_{gs\_ap}|/(n_{ap}+1)$. R_{opt_a} is given by $|V_{ap}|\ /|I_{ap}|$.

Step 2. Simulate the main PA at peak power: Set the drain bias voltage V_{DD_m} of the main PA and the gate bias at the threshold voltage V_T. Apply the fundamental drain RF voltage V_{mp} as shown in Fig. 2. Sweep the input gate voltage $|V_{gs\_mp}|$ at peak power to obtain $|I_{mp}|$.

Step 3. Simulate the main PA at backoff power: Set the drain bias voltage V_{DS_m} of the main PA and the gate bias V_{GG_m} at the threshold voltage V_T. Apply the fundamental drain voltage swing $V_{mb} = V_{mp}$ as shown in Fig. 2. The input gate voltage is set to $|V_{gs\_mb}| = |V_{gs\_mp}|/(n_m+1)$ at backoff power to obtain $|I_{mb}|$. Obtain the current ratio vector G_I=$|I_{mb}|/\ |I_{mp}|$ versus $|V_{gs\_mb}|$.

Step 4. Simulate the auxiliary PA at backoff power: Select n_{ab} of the auxiliary PA. Apply the fundamental drain voltage $|V_{ab}| = G_I|V_{ap}|$. Sweep the input gate voltage $|V_{gs\_ab}|$=$|V_{gs\_ap}|/(n_{ab}+1)$ to obtain $|I_{ab}|$ versus $|V_{gs\_ab}|$. (3) and (4) are solved given the 1D-swept data obtained from the 4 above steps.

Step 5. Simulate the intrinsic IV Doherty PA: The characteristic impedance Z_T and the common load R_L are calculated based on (5) and (6). The optimum RF gate voltage drives obtained in (4) are used with the intrinsic Doherty prototype synthesized in Steps 1-4.

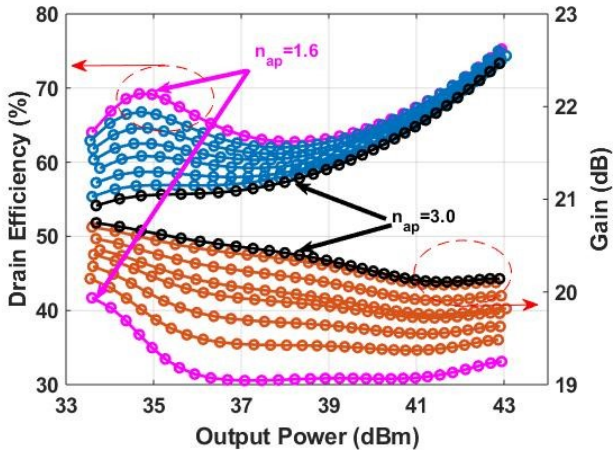

Fig. 3. Trade off between gain and drain efficiency

Step 6. Doherty combiner design at the package: The embedding device model used in [3] and [4] provides a direct way to build the output combiner by projecting the intrinsic currents and voltages to the package reference planes of the transistors. The two-port network parameters of the output combiner are synthesized using the method mentioned in [2]. Embedding process also generates the

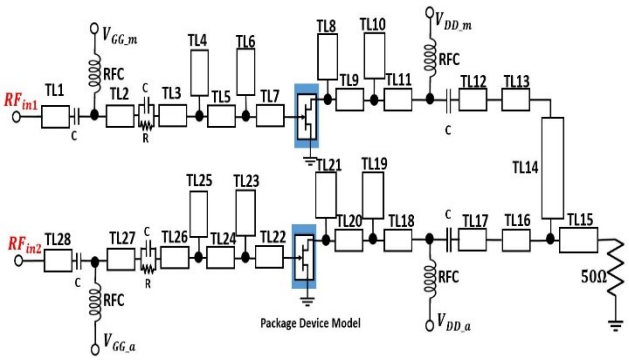

Fig. 4. Schematic of the asymmetric Doherty power amplifier circuits

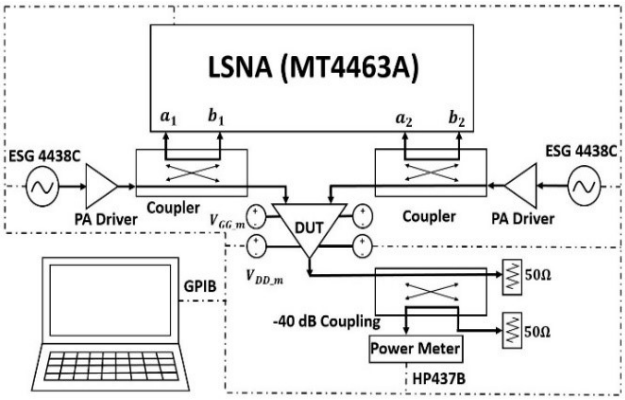

Fig. 5. Schematic of the large signal network analyzer (LSNA) testbed used for the CW measurements

optimal input and output harmonic impedances without using sourcepulls or loadpulls. In steps 1 to 4, n_{ap}, n_{ab}, and n_m are tunable asymmetry factors between the auxiliary and main amplifiers, which are defined by the ratio between the input voltage drives at peak power and backoff power level. They are all equal in the ideal case of constant g_m transistors. For single input Doherty PAs the input coupling ratio is constant, so it is necessary to select $n_{ab} = n_m$ to make $V_{gs\_ap}/V_{gs\_mp} = V_{gs\_ab}/V_{gs\_mb}$. This direct design algorithm is implemented in a Matlab code, which automatically calls ADS to perform harmonic balance simulations under script controls. Fig. 3 illustrates the Doherty gain-efficiency tradeoff by presenting the simulated results of multiple Doherty PA prototypes designed by using this automatic algorithm. By gradually decreasing n_{ap} from 3.0 to 1.6 and keeping $n_m = n_{ab} =$ 2.0, the efficiency increases as shown in Fig. 3, while the gain decreases and becomes more non-linear. In the next section n_{ap}=2.0 is selected. A dual input demonstrator asymmetric Doherty PA operating at 2 GHz is designed and fabricated to verify the algorithm. The schematic of the PA circuits is presented in Fig. 4.

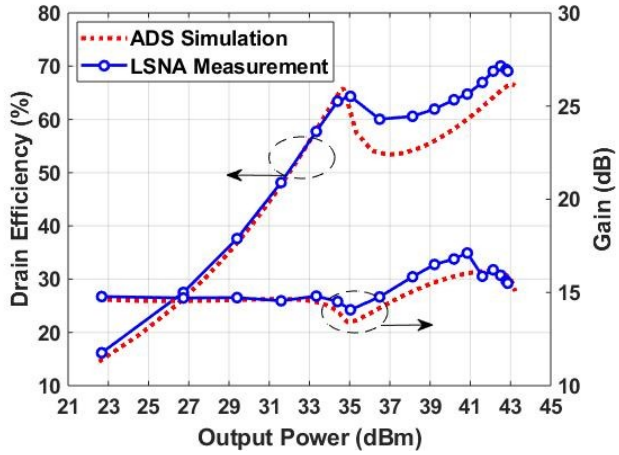

Fig. 6. Measured (blue dots) data and simulated (red dash) data at 2 GHz

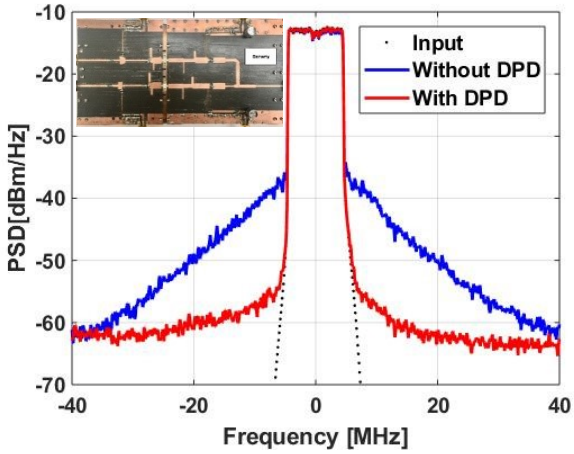

Fig. 7. Spectral density before (blue) and after (red) DPD and the fabricated Doherty PA

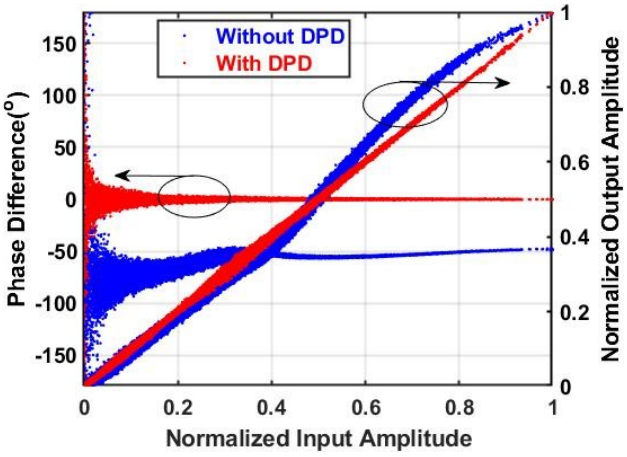

Fig. 8. AM/AM and AM/PM before (blue) and after (red) DPD

III. Measurement Results

A 2 GHz dual-input Doherty PA demonstrator circuit was designed using the automatic algorithm proposed in this paper and implemented on a RT/Duroid 5880 substrate with a relative dielectric constant of 2.2 and thickness of 31mil. Two Wolfspeed CGH27015 15-W GaN HEMT are used for the PA implementation. As shown in Fig. 5, the 90-degree phase offset and the incident power are digitally applied by using two RF source generators (ESG 4438C) at the dual-input of the fabricated Doherty PA in the CW measurements. Meanwhile, the output power are recorded by a power meter (HP 438B) and the DC consumptions are measured by using two DC supplies. Fig. 7 shows the fabricated Doherty PA board. The drain bias voltage and DC quiescent current for the main amplifier are 16 V and 55 mA, respectively. The auxiliary amplifier uses -3.8 V and 32 V for the gate and drain biases. In Fig. 6, the simulated data using Keysight ADS EM Co-simulation are compared with the measured data obtained from large signal network analyzer (LSNA) measurements. At 9 dB backoff power, the Doherty PA achieves about 63% drain efficiency. Meanwhile, the Doherty PA is able to deliver 42.9 dBm of maximum RF output power with a 69% drain efficiency. It is also noted that the measured gain is calculated by using the difference between the overall output power and the total input power added from both of the two input ports, which yields around 15 dB at 9 dB backoff. The dynamic response of the PA was tested with a 10 MHz LTE with 9.6 dB PAPR. The PA was then linearized with a simple digital pre-distortion technique. Fig. 7 shows the output spectra of the PA with and without DPD. Fig. 8 shows the amplitude-to-amplitude (AM/AM) and amplitude-to-phase (AM/PM) distortion with and without DPD, respectively. The modulated signal measurement results with the 10MHz LTE signals are summarized in Table 1.

IV. Conclusion

In this paper, a novel automatic design theory for Doherty PAs is introduced and demonstrated. By applying this automatic algorithm, multiple Doherty PAs at the intrinsic reference plane with different performances at the package reference planes are rapidly realized using non-linear embedding. This direct design method, which is implemented in an automatic algorithm, produces a functional DPA prototype in 95 seconds with a Linux workstation. A 2GHz dual-input Doherty PA was implemented and tested to validate the design methodology.

TABLE I
SUMMARY OF LINEARIZATION RESULTS

	P_{avg} (dBm)	DE_{avg} (%)	**ACLR** (dBc)	**NMSE** (dB)
Before DPD	33.5	52.4	-29.0	-0.758
After DPD	33.9	51.3	-45.5	-32.45

Acknowledgment

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