Flying capacitor multilevel PWM converter based UPFC

L. Xu and V.G. Agelidis

Abstract: A unified power flow controller (UPFC) based on the flying capacitor (FC) multilevel voltage-source converter (VSC) topology with phase-shifted sinusoidal pulse-width modulation (PWM) control is presented. This converter allows higher power handling, potentially lower power loss, lower harmonic distortion and hence less filtering requirements when compared with the typical two-level counterpart. The series converter injects a voltage with controlled magnitude and phase, to control the active/reactive power flow in a transmission line. The shunt converter absorbs/supplies active power demanded by the series converter to maintain a constant DC link voltage, also providing independent reactive support to the network. A complete model of the proposed UPFC system is shown and control circuits are described in the synchronous d - q frame. Finally, simulation results are provided to confirm the robustness of the proposed system.

1 Introduction

Demand for electrical energy continues to grow steadily in many countries. However, for various reasons, electricity grid upgrades, and especially the construction of new transmission lines cannot keep pace with such growing demands. Finding suitable rights-of-way is particularly difficult in the industrialised nations. This situation requires higher operating flexibility and better utilisation of the existing power lines. Flexible AC transmission systems (FACTS) employ state-of-the-art power electronics technology to electronically control the high-voltage side of the network. Specifically, they are capable of controlling the interrelated parameters that govern the operation of transmission systems including series impedance, shunt impedance, current, voltage, phase angle and oscillation damping and, therefore, increase power transmission capacity to its thermal limit [1–3].

The unified power flow controller (UPFC) [4, 5] is the 'ultimate' power electronic FACTS controller and should have the ability to handle relatively high power. The conventional two-level VSC requires a large number of power devices connected in series, and/or parallel, and considerable high switching frequency has either to be used in order to reduce the harmonic distortion to acceptable levels, or else to use relatively large filter elements. This, in turn, gives rise to high power switching losses in the converter. One solution to high-power application is the use of multilevel VSCs, which allows higher power handling capability with reduced harmonic distortion and lower switching power losses when compared with its two-level

counterpart. Cascaded multimodular VSCs via a connection transformer [6, 7], and diode-clamped multilevel VSCs [8, 9] have already been proposed for UPFC applications. In [10] a matrix converter topology was explored. On the other hand, in [11, 12], a new multilevel converter topology, the so-called flying capacitor (FC) multilevel VSC was introduced. It uses a phase-shifted sinusoidal PWM strategy to control the individual switches and is capable of generating multilevel voltage waveforms with reduced power loss within the converter, lower total harmonic distortion and increased bandwidth when compared with a conventional two-level system. Therefore, this converter topology could be an ideal candidate for high-power applications. However, apart from a few notable papers such as in reference [13] where it was used for a shunt connected power line conditioner, no work has been reported on the potential application of the said topology as a UPFC.

The objective of this paper is to present an investigation of a UPFC based on the flying capacitor multilevel VSCs with phase-shifted sinusoidal PWM control. The system uses IGBT technology, and, due to the multilevel structure, the resultant output voltage can have very high-frequency harmonics, although the actual switching frequency of the individual switches is kept relatively low. This depends upon the level of the converter used to build the UPFC. A synchronous d - q reference-frame-based model of a UPFC is derived and control circuits are presented. Finally, simulation results are presented to show the flexibility and performance of the proposed system.

2 System configuration

The system configuration of a typical UPFC is shown in Fig. 1. It consists of two VSCs of which one is connected in shunt and the other in series. They are operated from a common DC link. The series converter performs the main function of the UPFC by injecting an AC voltage with controllable magnitude and phase angle in series with the transmission line, via series connected transformers.

The basic function of the shunt converter is to supply/absorb the active power demanded by series one at the common DC link, and thus maintain a constant DC link voltage. Furthermore, it can also be used to generate/absorb

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IEE Proceedings online no. 20020374

DOI: 10.1049/ip-epa:20020374

Paper first received 30th October 2001 and in revised form 6th March 2002

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Fig. 1 System configuration of a UPFC based on VSCs

controllable reactive power and provide independent shunt reactive compensation for the transmission line. The series converter supplies/absorbs the reactive power locally and exchanges active power with the shunt converter via the common DC busbar.

For the proposed UPFC system, each VSC shown in the generic diagram of Fig. 1 consists of a three-phase five-level flying capacitor multilevel VSC. For clarity, Fig. 2 shows one of its legs of the said converter. As it is shown, for a five-level system, apart from the DC link capacitor, there are three sets of flying capacitor banks with voltages charged at $V_{dc}/4$, $V_{dc}/2$ and $3V_{dc}/4$, respectively. As a result, the voltage across each switch is only a quarter of the DC link voltage. This simplifies the design of the series-connected IGBT stack compared to the conventional two-level VSC in which the voltage across each switch equals the DC link voltage. Furthermore, Fig. 3 shows the output line-to-line voltage waveform and the corresponding spectrum under phase-shifted sinusoidal PWM control scheme [13]. With the carrier frequency and the switching frequency of individual switches being 1 kHz, it clearly shows that the dominant harmonics of the output voltage are positioned around 4 kHz and multiples thereof as the theory suggests. The multiplier factor of four is due to the five-level converter considered which requires four triangular carriers of the same frequency (1 kHz) and phase-shifted by one fourth of the carrier period. This dramatically reduces the switching power loss compared to a two-level VSC, if similar output harmonic distortion is to be achieved. Alternatively, if similar power loss is to be maintained, the proposed system requires smaller size filters when compared to a two-level VSC.

Fig. 2 Phase leg of a 5-level flying capacitor multilevel VSC

Fig. 3 Output line-to-line voltage waveform (volts) and the corresponding spectrum
Switching frequency $f_{sw} = 1$ kHz

Although the voltage harmonics of the proposed UPFC system are at high frequencies, a filter may still be needed to reduce the harmonic interaction and telephone interference. A high-frequency filter can be inserted between the VSC and the transformer for both the series and shunt converters. The filter simply comprises a series reactor and shunt capacitor and is tuned at 4 kHz. Fig. 4a shows it as a single line diagram. The resistor R provides the necessary damping. This high-frequency filter also reduces the dv/dt applied to the transformer, otherwise a special transformer has to be designed for the application. If a 2-level VSC and same switching frequency of 1 kHz are used, the dominant harmonics are around 1 kHz and 2 kHz, with much higher amplitude than the 5-level flying capacitor VSC. Two shunt elements may be needed with one tuned at 1 kHz and the other tuned at 2 kHz as shown in Fig. 4b. The operating conditions, the AC source impedance range and other factors determine the electrical ratings of the filter components. In general, comparing the two high-frequency filter designs, the filter for the proposed five-level flying capacitor VSC can be many times smaller than the filter for two-level VSC. This is due to the fact that not only the harmonic frequency is higher, but also the harmonic amplitude is lower, for the five-level flying capacitor VSC.

Fig. 4 Single-line diagrams

a high frequency (HF) filter for the 5-level flying capacitor VSC (switching at 1 kHz) tuned at 4 kHz
b HF filters for the 2-level VSC (switching at 1 kHz) tuned at 1 kHz and 2 kHz, respectively

3 Operating modes of a UPFC

Control of transmission line parameters and transmitted active and reactive power are achieved by inserting a voltage vector V_c via the series converter to the input terminal voltage, as shown in Fig. 1. By appropriate control of V_c the UPFC can be used to fulfill different control objectives. As it has been shown in [1], [4] and [14], the basic operation mode of a UPFC can be identified as follows:

- (i) *Shunt compensation only:* The series element of the UPFC is disabled and it acts as a STATCOM;
- (ii) *Terminal voltage regulation only:* V_c is injected in phase with V_s to compensate voltage amplitude;
- (iii) *Terminal voltage regulation and series line compensation:* V_c is injected to compensate voltage amplitude and it also contains a voltage component which is in quadrature with the line current I_s ;
- (iv) *Terminal voltage and phase angle regulation:* V_c is injected to achieve the desirable voltage amplitude and phase angle with respect to the source voltage V_s ;
- (v) *Power flow control:* The magnitude and angular position of the injected voltage V_c are fully controlled, to control the active and reactive power flow in the transmission line, to satisfy load demand and system operating conditions.

As power flow control is the ultimate objective of a UPFC and many studies have already been conducted on series voltage and phase angle regulation [15, 16], this paper will focus on the investigation of a UPFC for power flow control and shunt compensation.

4 Modeling and control of a UPFC

A UPFC system can be divided into two subsystems, i.e. shunt and series elements, which are linked together by a common DC link for active power exchange. Hence, the modelling of a UPFC system is divided into three parts, namely shunt, series and the DC link circuit.

Assuming the transmission system is symmetrical, the modelling process is then conducted in the synchronous $d-q$ reference frame. The three-phase variables are transformed into the $d-q$ reference frame using Park transformation. Neglecting the source impedance X_s , the equivalent circuit of the shunt converter connected to the network is shown in Fig. 5, where the voltage sources V_{ps} and V_p represent the output of the shunt transformer and the shunt converter, respectively. ω is the source angular frequency and the parameters L_p and R_p represent the leakage inductance and resistance of the shunt transformer and any other reactors connected, respectively.

Fig. 5 Equivalent circuit of the shunt element in the synchronous $d-q$ frame

According to Fig. 5, in the $d-q$ frame the shunt circuit can be expressed by the following differential equation

$$\frac{d}{dt} \begin{bmatrix} i_{pd} \\ i_{pq} \end{bmatrix} = \begin{bmatrix} -\frac{R_p}{L_p} & \omega \\ -\omega & -\frac{R_p}{L_p} \end{bmatrix} \begin{bmatrix} i_{pd} \\ i_{pq} \end{bmatrix} + \frac{1}{L_p} \begin{bmatrix} v_{pd} - V_{ps} \\ v_{pq} \end{bmatrix} \quad (1)$$

Similarly, the equivalent circuit of the series element is shown in Fig. 6 where the series converter output is represented by a voltage source V_c . The system can be expressed as

$$\frac{d}{dt} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} -\frac{R_c}{L_c} & \omega \\ -\omega & -\frac{R_c}{L_c} \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \frac{1}{L_c} \begin{bmatrix} v_{cd} + V_s - v_{rd} \\ v_{cq} - v_{rq} \end{bmatrix} \quad (2)$$

Fig. 6 Equivalent circuit of the series element in the synchronous $d-q$ frame

As it has been described previously, the two converters exchange active power via the DC link and the DC link voltage is determined by the active power flow between the AC and DC side via the shunt and series converters. Fig. 7 shows the equivalent circuit of the active power flow, where resistor R_c is used to represent the power losses in the two converters and C is the value of the DC link capacitor. According to Figs. 5 and 6 and neglecting the power loss on the resistor R_p , the active power flows from the AC side into the DC side by the shunt and series converters can be expressed as

$$p_{shunt} = -\frac{3}{2} V_{ps} \cdot i_{pd}$$

$$p_{series} = \frac{3}{2} (v_{cd} \cdot i_{sd} + v_{cq} \cdot i_{sq}) \quad (3)$$

Based on Fig. 7 and (3), the DC link voltage can be expressed as

$$\frac{d}{dt} [V_{dc}] = \left[-\frac{1}{R_c C} \right] \cdot [V_{dc}] + \frac{3}{2C} \left[-\frac{V_{ps}}{V_{dc}} \cdot i_{pd} + \frac{v_{cd} \cdot i_{sd} + v_{cq} \cdot i_{sq}}{V_{dc}} \right] \quad (4)$$

Fig. 7 Equivalent circuit of the AC/DC active power flow

As determined by (1) and (2), the dynamic characteristics of the shunt and series converters are mainly determined by

R_p/L_p and R_c/L_c , respectively. As it has been shown in [17], because of the relatively small value of R_p/L_p and R_c/L_c compared to ω , the crossing-gain, defined as the gain from d -axis voltage to q -axis current (or gain from q -axis voltage to d -axis current) is much greater than the direct gain which is defined as the gain from d -axis voltage to d -axis current (or q -axis voltage to q -axis current). The steady-state d - and q -axis currents are predominately controlled by the q - and d -axis voltages, respectively. As a result, the crosscoupling control method [17] is superior to decoupling control which is used in [18]. In [19, 20], the crosscoupling control method presented in [17] was modified to reduce the power fluctuation and, therefore, to improve the transient stability. The control strategy used for the series converters in this investigation is mainly based on the control method presented in [17] and [19, 20]. While for the shunt converter, the main emphasis is on the DC link voltage control, which was not studied in [17] or [19, 20].

According to (1) and (2), the reference voltages of the series and shunt converters in the d - q frame are then given, respectively, by

$$\begin{bmatrix} v_{cd}^* \\ v_{cq}^* \end{bmatrix} = \begin{bmatrix} k_1 & -(k_{p1} + \frac{k_{i1}}{S}) \\ k_{p2} + \frac{k_{i2}}{S} & k_1 \end{bmatrix} \begin{bmatrix} i_{sd}^* - i_{sd} \\ i_{sq}^* - i_{sq} \end{bmatrix} + \begin{bmatrix} -V_s + V_{rd} \\ V_{rq} \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} v_{pd}^* \\ v_{pq}^* \end{bmatrix} = \begin{bmatrix} k_2 & -(k_{p3} + \frac{k_{i3}}{S}) \\ k_{p4} + \frac{k_{i4}}{S} & k_2 \end{bmatrix} \begin{bmatrix} i_{pd}^* - i_{pd} \\ i_{pq}^* - i_{pq} \end{bmatrix} + \begin{bmatrix} V_{ps} \\ 0 \end{bmatrix} \quad (6)$$

where k_1 and k_2 act as damping resistors [19, 20].

Assuming the voltage amplitude and phase differences between the sending and receiving ends are small, (5) can be approximated as

$$\begin{bmatrix} v_{cd}^* \\ v_{cq}^* \end{bmatrix} = \begin{bmatrix} k_1 & -(k_{p1} + \frac{k_{i1}}{S}) \\ k_{p2} + \frac{k_{i2}}{S} & k_1 \end{bmatrix} \begin{bmatrix} i_{sd}^* - i_{sd} \\ i_{sq}^* - i_{sq} \end{bmatrix} \quad (7)$$

As the DC link voltage is controlled by the d -axis current i_{pd} of the shunt converter, i_{pd}^* is then given by

$$i_{pd}^* = -X_3 + \frac{v_{cd} \cdot i_{sd} + v_{cq} \cdot i_{sq}}{V_{ps}} \quad (8)$$

where

$$X_3 = \left(k_{p5} + \frac{k_{i5}}{S} \right) \cdot (V_{dc}^* - V_{dc}) \quad (9)$$

As the value of v_{cd} and v_{cq} are not directly available to the control system, they are approximated by their reference values of v_{cd}^* and v_{cq}^* , respectively. This is based on the fact that, with PWM control, the response of the converter output voltage can be instantaneous (with one switching period delay). Therefore, (8) can be rewritten as

$$i_{pd}^* = -X_3 + \frac{v_{cd}^* \cdot i_{sd} + v_{cq}^* \cdot i_{sq}}{V_{ps}} \quad (10)$$

According to (6), (7), (9) and (10), the block diagram of the control circuits for a UPFC is shown in Fig. 8. It combines the control circuits for both series and shunt converters. As it is shown, the three-phase currents of the shunt and series converters are measured and transformed into the synchronous d - q reference frame fixed to the source voltage vector V_s using the information of $\sin \omega t$ and $\cos \omega t$ generated by the phase locked loop (PLL). The shunt converter controls the active power flow into the DC link capacitor, which is determined by the q -axis voltage component v_{pq} to maintain a constant DC link voltage. Furthermore, according to the reactive power demand, it also provides independent shunt reactive compensation for the transmission line, which is determined by the d -axis voltage component v_{pd} . Two PI regulators are used to generate the desirable d - and q -axis voltage components. The main task of a UPFC, i.e. active and reactive power flow control, is accomplished by the series converter. As Fig. 8 shows, the d - and q -axis current references generated from the active and reactive power demands are compared with the measured values. Again, two PI regulators are used to produce the d - and q -axis voltage references, while gain k_1 acts as a damping resistor. The d - and q -axis voltage references, for the shunt and series

Fig. 8 Block diagram of the control circuit

converters are then transformed back to the stationary three-phase quantities and fed to their respective SPWM modulators to generate appropriate gate signals to control the operation of the two flying capacitor multilevel VSCs.

5 Simulation results

System simulations were carried out using the well-known software programme SABER [21]. During the simulation, phase-shifted SPWM was used with the carrier and switching frequencies being equal to 1 kHz. Owing to the use of five-level flying capacitor VSC, although the switching frequency is 1 kHz, the bandwidth of the control system, which is normally limited by the equivalent switching frequency, can be as high as 4 kHz. The sending- and receiving-end busbar voltages are assumed to be constant, of the same amplitude of 10 kV (peak) and displaced by an angle of 15° . The output voltage of the shunt transformer is 3.75 kV (peak). The series inductance and resistance are 0.1 p.u. and 0.01 p.u., respectively (10 kV, 30 MVA, 50 Hz base). For the shunt circuit, the inductance and resistance are 0.28 p.u. and 0.03 p.u., respectively. A relatively large DC capacitor of 2000 μ F is used due to the large power demanded by the series converter at some operating conditions. However, the capacitances for the flying capacitors are set at 200 μ F. This is due to the factor that, for the FC multilevel VSC, the voltage of each flying capacitor is balanced within each switching cycle; therefore, relatively small capacitors can be used. As the control strategy adopted is based on crossing-coupling control [17], relatively small gains have been used for both the shunt and series converters. The parameters of the control system are listed in Table 1.

Table 1: Parameters of the control circuits

k_1	k_{p1}	k_{p2}	k_{p3}	k_{p4}	k_{p5}
3.3	0.5	0.5	1	6	0.5
k_2	k_{i1}	k_{i2}	k_{i3}	k_{i4}	k_{i5}
6	500	500	500	500	50

System start of the shunt converter was simulated first and then reactive reversal was examined. Before the system starts, it is assumed that the DC link capacitor and the individual flying capacitors of the multilevel VSC have been initially charged to their desired values. Although the initial charging of the flying capacitors is a challenge and important for the functioning of this converter, further information can be found in [22]. Figs. 9 and 10 show the simulated waveforms when the shunt system started with the reference reactive power being +2.5 MVar and -2.5 MVar, respectively. Fig. 11 shows the waveforms during reactive reversal. The responses are quite satisfactory for both start and reactive reversal, although relatively small gains have been used for the controller. The response time is normally within one fundamental cycle and the fluctuation of the reactive power is small, largely due to the existence of k_2 acting as a damping resistor. The DC voltage is well controlled with a small ripple.

The simulated results of power flow control by the UPFC system are shown in Fig. 12 for $P^* = 30$ MW, $Q^* = 0$ MVar, in Fig. 13 for $P^* = 20$ MW, $Q^* = 10$ MVar, and in Fig. 14 for $P^* = 20$ MW, $Q^* = 10$ MVar, respectively. As shown, after the series element of the UPFC is

Fig. 9 Simulated results of the UPFC shunt converter operation for $Q_p^* = 2.5$ MVar

Q_p = reactive power, MVar (dash line = reference, solid line = response); V_{dc} = DC link voltage (10 kV); v_{psa} = phase A source voltage, V; i_{par} = phase A line current, A (switching frequency $f_{sw} = 1$ kHz, source voltage $V_s = 3.75$ kV $\angle 0^\circ$ (peak), nominal DC link voltage $V_{dc} = 10$ kV)

Fig. 10 Simulated results of the UPFC shunt converter operation for $Q_p^* = -2.5$ MVar, system start

started at the time of 0.15 s, the active and reactive power flows were quickly restored to the reference values and fully controlled by the UPFC. The response time again is within one fundamental cycle and the power fluctuation is small.

The DC voltage control of the shunt converter during transient operation of the series converter was tested and Fig. 15 shows the simulated results. After the series converter started at 0.15 s, the transmitted active and reactive powers are quickly restored to their reference value, while the current of the shunt converter responds accordingly to maintain a constant DC link voltage. As the series converter absorbs active power at this operating mode (and indeed it has to be fed back to the network by the shunt converter), the phase angle between the shunt current and voltage becomes less than 90° . This indicates active power transmitted from the DC side back to the AC side by the shunt converter that provides independent reactive power support of +2.5 MVar.

Fig. 11 Simulated results of the UPFC shunt converter operation for reactive reversal (Q_p dash line=reference, Q_p solid line=response)

Fig. 12 Simulated results of the UPFC series converter operation $P^*=30$ MW, $Q^*=0$ MVar

P =active power flow (MW); Q =reactive power flow (MVar); v_{cu} =phase A inserted series voltage, V; v_{st} =phase A sending-end source voltage, V; I_{sa} =phase A line current, A (switching frequency $f_{sw}=1$ kHz, sending-end voltage $V_s=10$ kV $\angle 0^\circ$ (peak), receiving-end voltage $V_r=10$ kV $\angle -15^\circ$ (peak), nominal DC link voltage $V_{dc}=10$ kV).

Fig. 13 Simulated results of the UPFC series converter operation for $P^*=20$ MW, $Q^*=+10$ MVar

Fig. 14 Simulated results of the UPFC series converter operation for $P^*=20$ MW, $Q^*=10$ MVar.

Fig. 15 Simulated results of UPFC operation

Q_p =reactive power by the shunt converter (2.5 MVar); P =active power flow (20 MW); Q =reactive power flow (10 MVar); V_{dc} =DC link voltage (10 kV); v_{st} =sending-end phase A source voltage V; I_{sa} =shunt converter phase A current (A); I_{sa} =phase A line current, A (switching frequency $f_{sw}=1$ kHz, sending-end voltage $V_s=10$ kV $\angle 0^\circ$ (peak), receiving-end voltage $V_r=10$ kV $\angle -15^\circ$ (peak), nominal DC link voltage $V_{dc}=10$ kV)

6 Conclusions

The possibility of using flying capacitor multilevel PWM converters for a UPFC application is discussed. The new UPFC generates output voltage waveforms with lower harmonic distortion, when compared with the typical topology, based on the two-level VSC due to the multilevel nature of the system, and allows higher power handling capability. In the synchronous reference frame, a complete model of a UPFC has been presented and control circuits for both the shunt and series converters have been described. The simulated results presented confirm that

the performance of the proposed UPFC is satisfactory for active/reactive power flow control and independent shunt reactive compensation.

7 Acknowledgment

The authors would like to acknowledge the financial support provided by the Scottish Higher Education Funding Council (SHEFC), through a grant for the establishment of the Inter-University Glasgow-Strathclyde Centre for Economic Renewable Power Delivery (CERPD).

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