

AMS 0.18 μm PDK Setup and Cadence Tutorial

Contributors

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AMS 0.18 μm PDK Setup

Step 1: First Time Use Instructions:

If you have never set up this PDK before, you will need to go through this step. If you have already gone through this step once before, please skip to step 2.

- Log in to one of the following servers (rh053, rh054, or rh055). Please note that these are the only servers you can use for the AMS 0.18 μm PDK
- From the Desktop, open a new Terminal (Applications >> System Tools >> Terminal)
- In your home directory, create a new directory called “cadence” (mkdir cadence). If you already have a “cadence” directory, then ignore this step.
- Change directory to “cadence” (cd cadence), then create a new directory called “AMS18” (mkdir AMS18)
- Change directory to “AMS18” (cd AMS18)
- Execute the following commands in sequence:
 - source /data/design_kits/ForUsers/AMS/startup.ams
 - source /data/design_kits/ForUsers/launch.cad616

```
[fayed.1@rh053 ~]$ mkdir cadence
[fayed.1@rh053 ~]$ cd cadence
[fayed.1@rh053 ~/cadence]$ mkdir AMS18
[fayed.1@rh053 ~/cadence]$ cd AMS18
[fayed.1@rh053 AMS18]$ source /data/design_kits/ForUsers/AMS/startup.ams
[fayed.1@rh053 AMS18]$ source /data/design_kits/ForUsers/launch.cad616
Starting Cadence 6.1.6 environment set-up...
```

```
Warning: cds.lib file not found in /rcc4/homes/fayed.1/cadence/AMS18 directory.
This directory may not be appropriate for launching CDS tools...
```

```
Warning: .cdsinit file not found in /rcc4/homes/fayed.1/cadence/AMS18 directory.
This directory may not be appropriate for launching CDS tools...
```

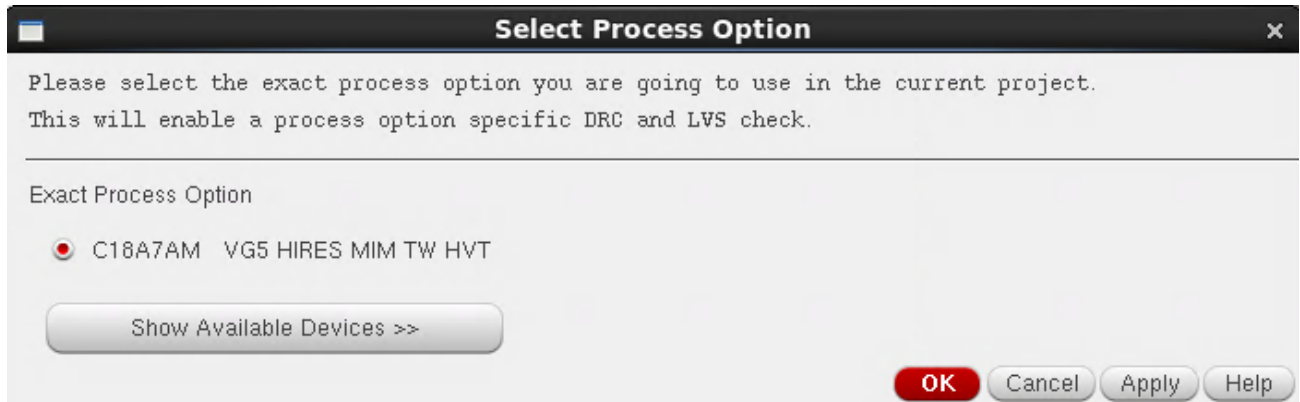
```
.cdsenv file not found but may be generated automatically...
```

Note: For NC-SystemC compiles use variables found in /data/cadence/IUS82/tools/systemc/files/make

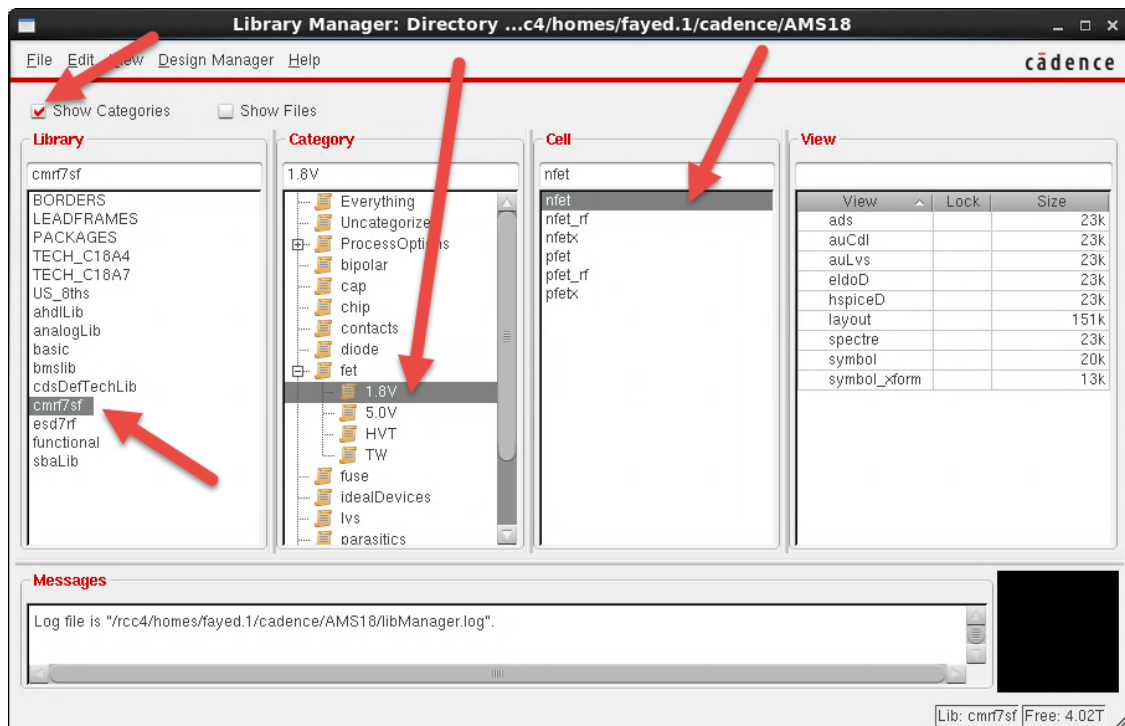
Configuring Mentor Graphics Calibre 2014.2_33 environment:

```
Setting Calibre, version 2014.2_33.25
PATH updated
[fayed.1@rh053 AMS18]$ █
```

- Start Cadence by executing the following command:
 - `ams_cds -tech c18a7`
- The following Virtuoso window will appear. Just click “OK”.



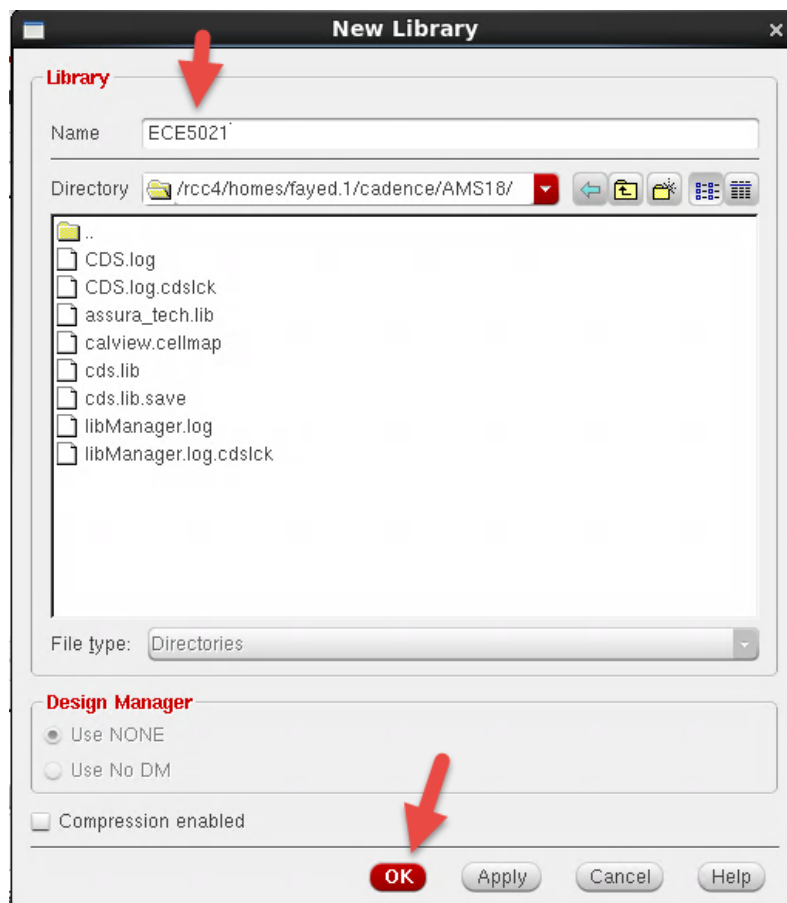
- Cadence Library Manager window will also appear. Under the “Library” column, the library called “cmrf7sf” contains all the devices in AMS 0.18 μm process. Select that library, then check “show categories”. Under the “category” column, select the type of devices you want to see (for example expand “fet” and then select “1.8V”). All the devices under that specific category will be listed under the “Cell” column. Select the specific devices you want, and you will see the different views available for that device (schematic, symbol, etc..) listed under the “View” column. If you want to see everything in the library regardless of the device type, just select the “Everything” category.



Step 2: Creating a Library for your own Project/Class:

If you have already set up the PDK once before (by going through step 1), you will need to go through this step to create a library for your specific project or class. You will need to go through this step every time you want to create a NEW library (for instance if you are starting a new project or a new class). If your library already exists (you created it once before by going through this step), you can skip to step 3.

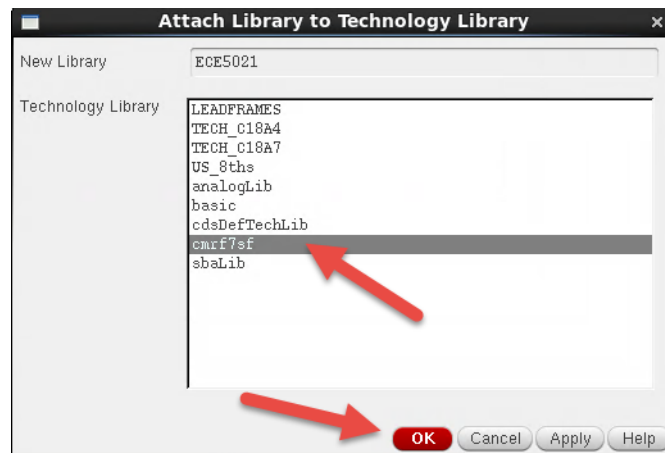
- Log in to one of the following servers (rh053, rh054, or rh055). Please note that these are the only servers you can use for the AMS 0.18 μ m PDK
- From the Desktop, open a new Terminal (Applications >> System Tools >> Terminal)
- Change directory to “AMS18” (cd ~/cadence/AMS18)
- Execute the following commands in sequence:
 - source /data/design_kits/ForUsers/AMS/startup.ams
 - source /data/design_kits/ForUsers/launch.cad616
 - ams_cds -tech c18a7
- In the library manger, go to the menu “File >> New >> Library”
- Type the desired name of your new library, for example “ECE5021”. Leave the directory at the default, then click OK.



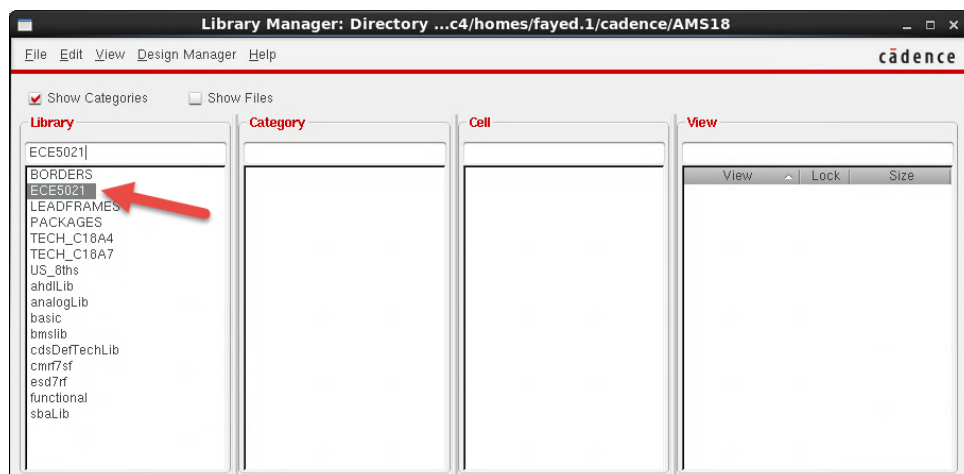
- The following window will now appear. Make sure you select “Attach to an existing technology library”, then click ok



- The following window will now appear. Make sure you select “cmrf7sf”, then click ok



- Now the Library Manager will show the library you just created (and other libraries you may have created in the past)



Step 3: Routine Use Instructions:

If you have already set up the PDK once before (by going through step 1), and created a library for project/class (by going through step 2), you need to go through this step every time you want to start Cadence and use the PDK:

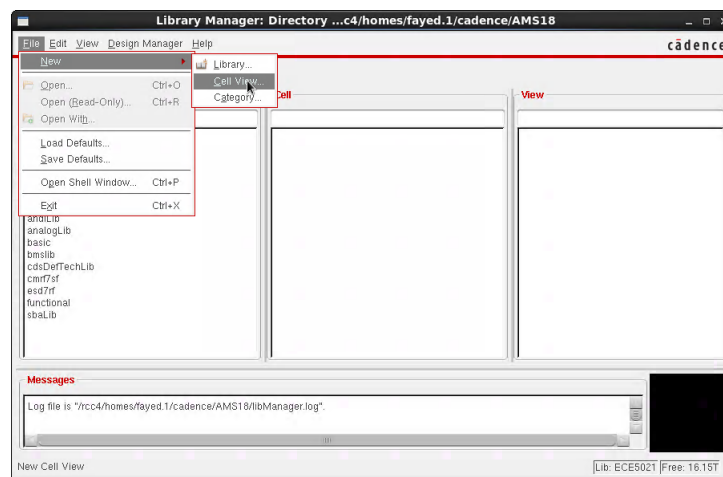
- Change directory to “AMS18” (cd ~/cadence/AMS18)
- Execute the following commands in sequence:
 - source /data/design_kits/ForUsers/AMS/startup.ams
 - source /data/design_kits/ForUsers/launch.cad616
 - ams_cds -tech c18a7

Cadence Tutorial using AMS 0.18 μm PDK

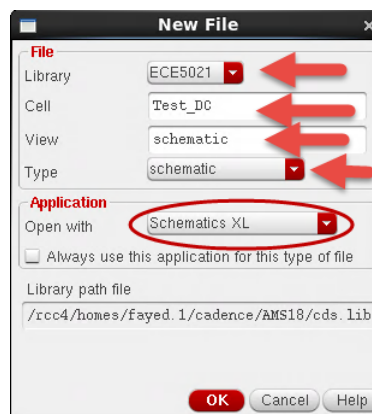
DC Simulations:

In this part, you will learn how to run DC simulations to plot I_D versus V_{DS} of an NMOS transistor in the AMS 0.18 μm PDK.

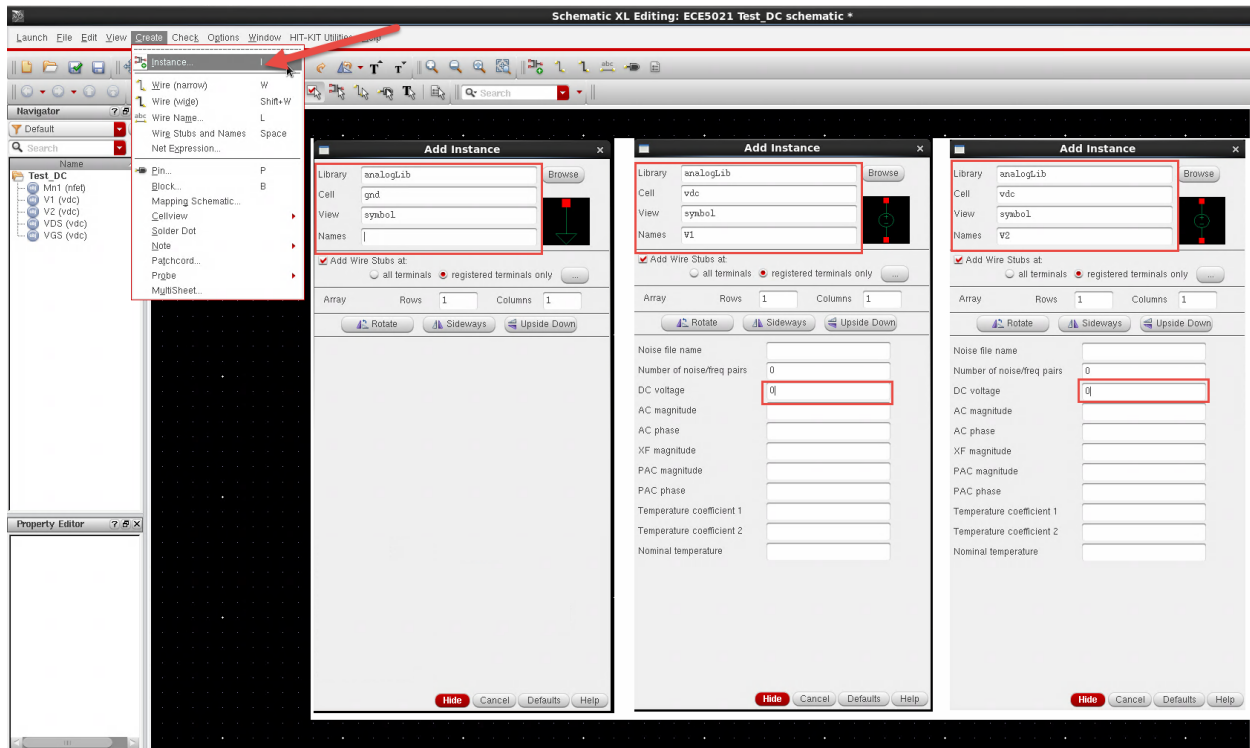
- Start Cadence by following step 3 of the PDK setup instructions (assuming you have gone through steps 1 and 2 at least once before)
- In the Library Manager, select the library you created in step 2 of the PDK setup instructions, or whatever library you created in the past and would like to use. Create a new cell view by going to “File >> New >> Cell View”



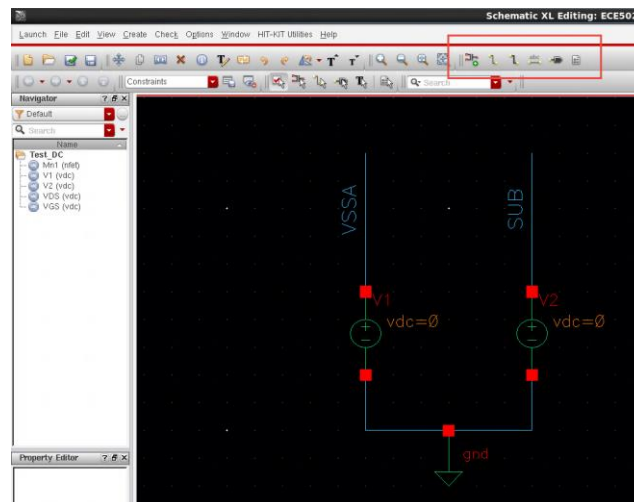
- The following window will appear. Fill in the fields as shown and click ok



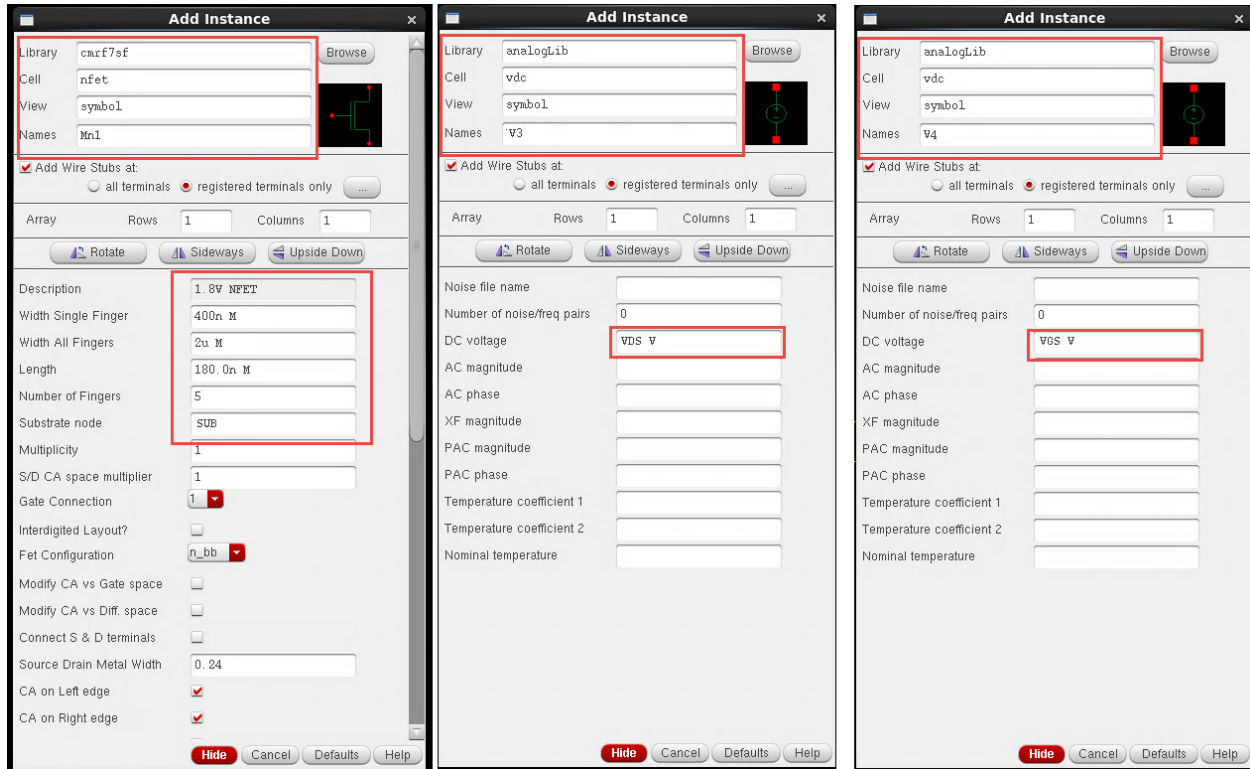
- A blank schematic window will appear as shown below. Use the “Create>>Instance” menu to instantiate a new component. You can also simply use the shortcut “i”. An add instance window will appear. Browse for each component shown below and enter its parameters as shown below and click hide. You will only be able to instantiate one component at a time.



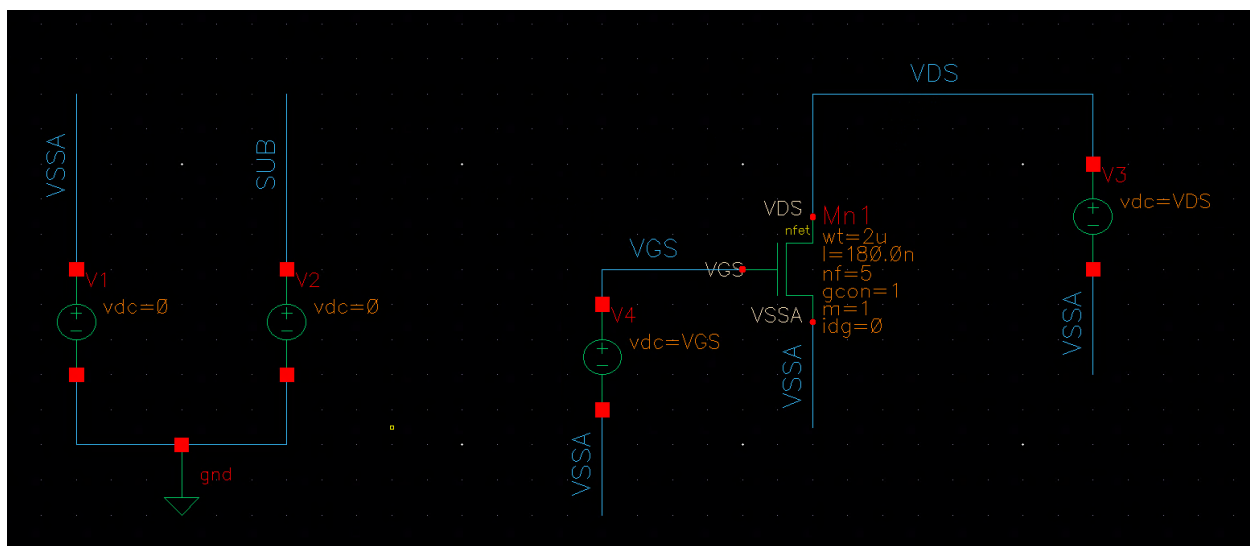
- Using the shortcuts at the top of the schematic window, connect the voltage sources and ground and name the wires as shown below



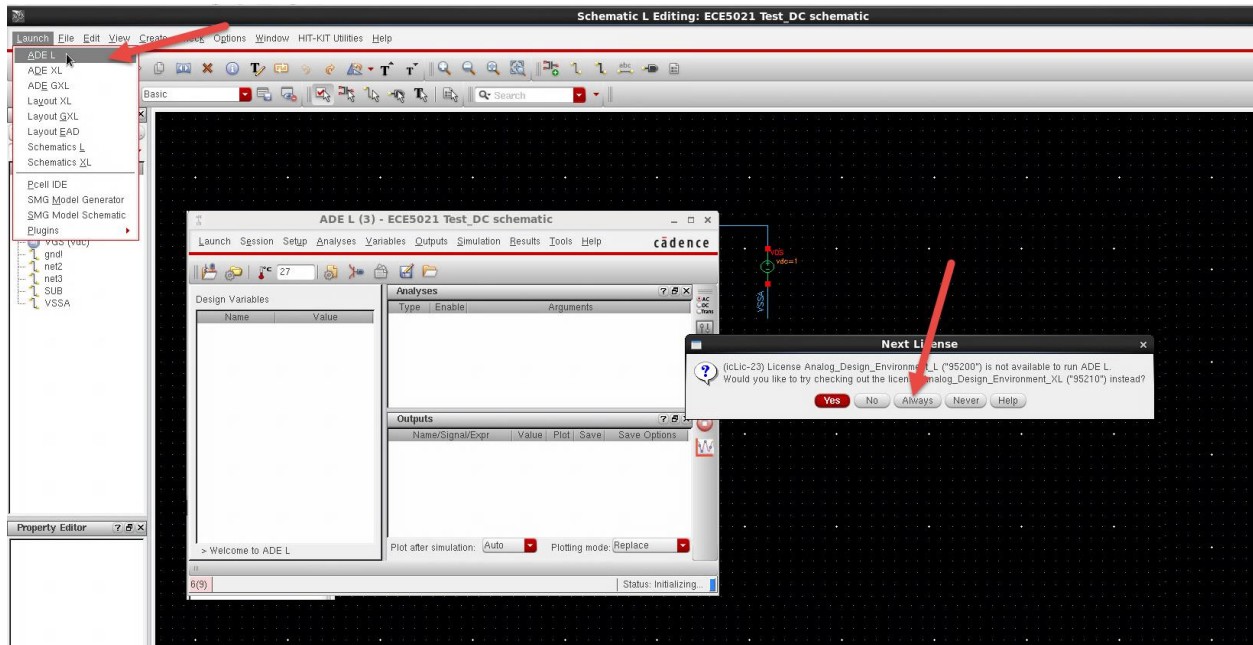
- Use the “Create>>Instance” menu to instantiate an NMOS transistor. Browse of the NMOS transistor in the PDK and enter its parameters as shown below. Instantiate two more voltage sources for VGS and VDS as shown below.



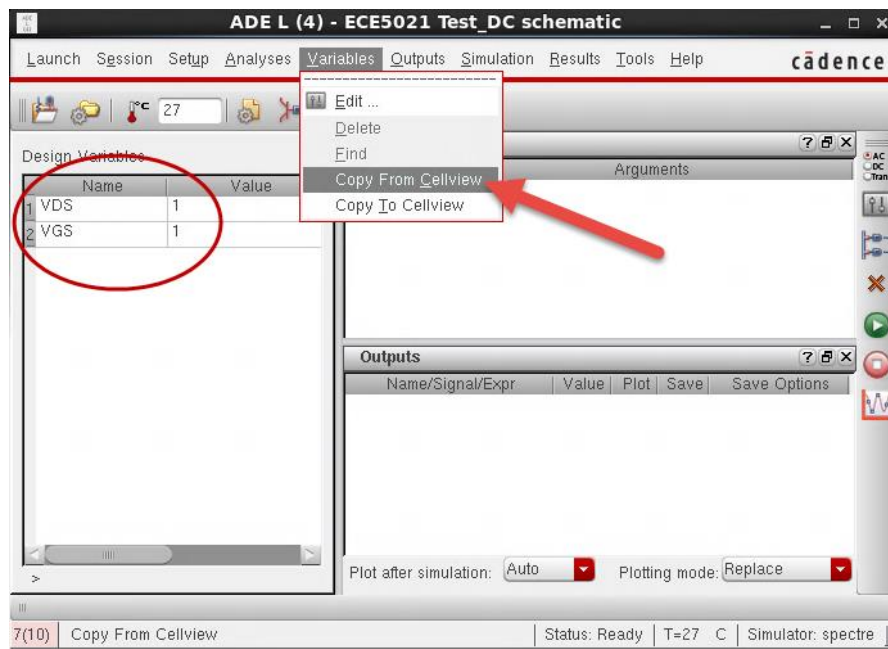
- Connect all the components as shown below



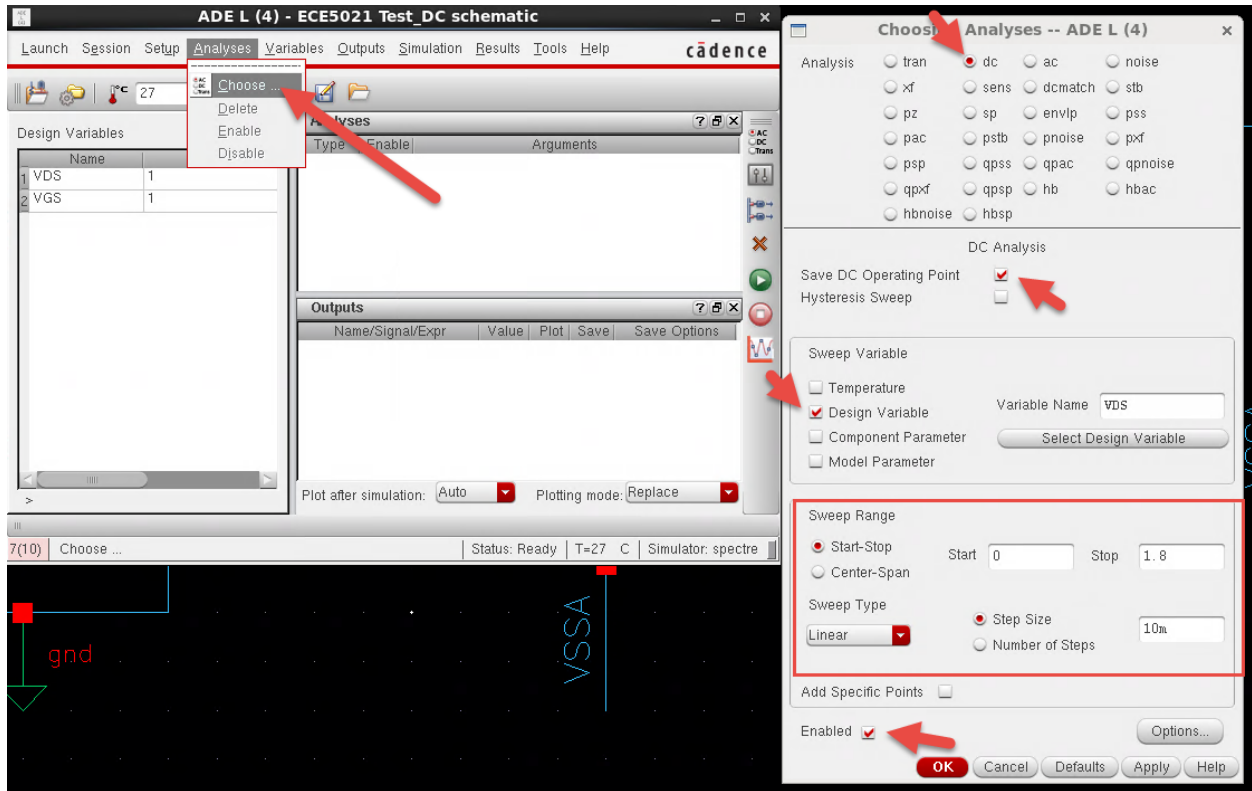
- Start the Analog Design Environment (ADE L) as shown below



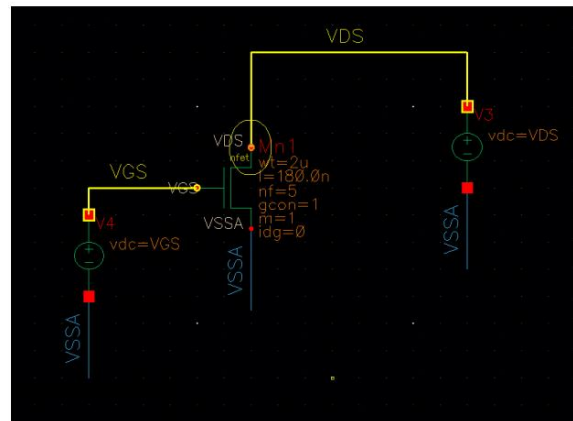
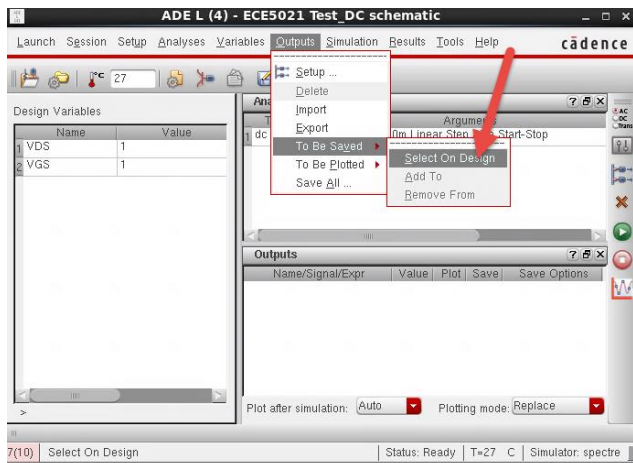
- To set VGS and VDS, use the menu "Variables>>Copy from Cell View" to bring in these parameters from the schematic to ADE L. They will appear under Design Variables. You can set them to any value you like by double clicking each parameter



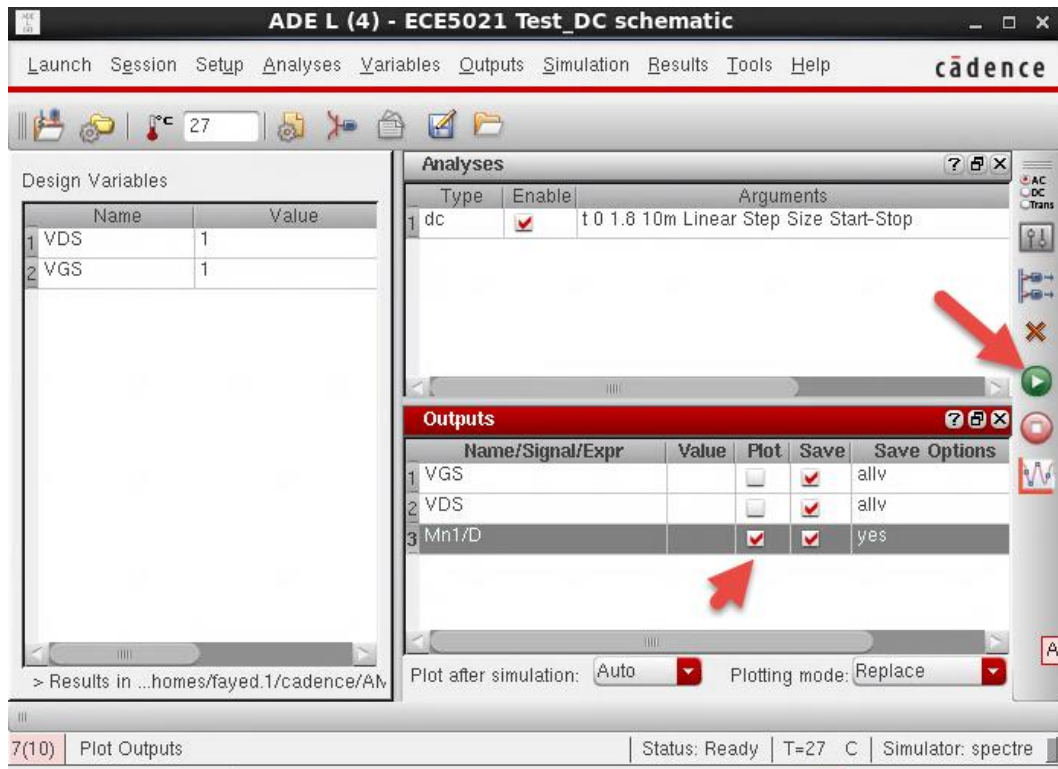
- Set up the DC analysis as shown below and click ok



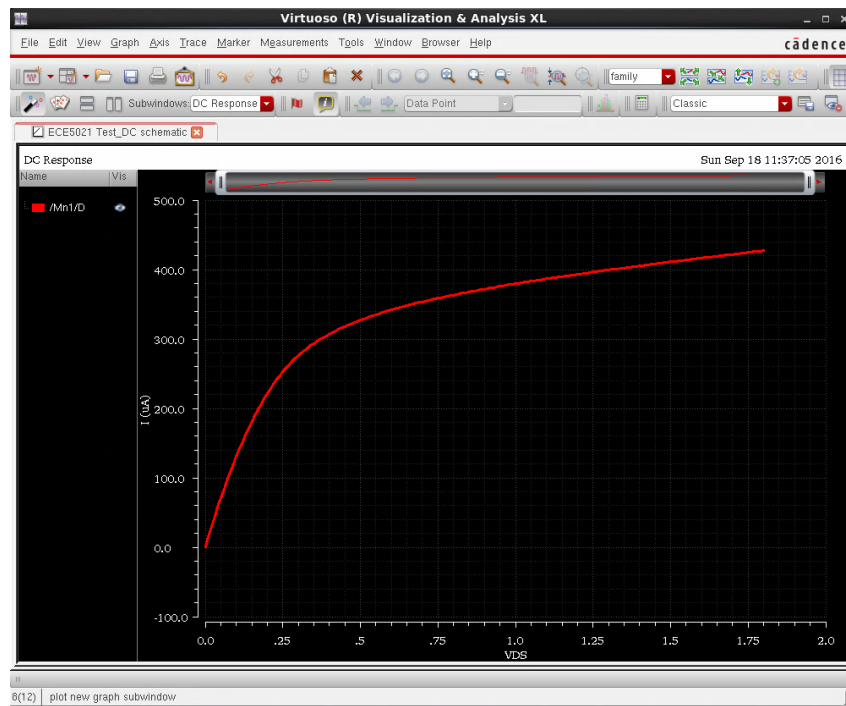
- Choose the signals that you need to be saved by selecting the desired wires and terminal currents on the schematic as shown below.



- Select the signals you want to plot, then start the simulation by clicking the play button



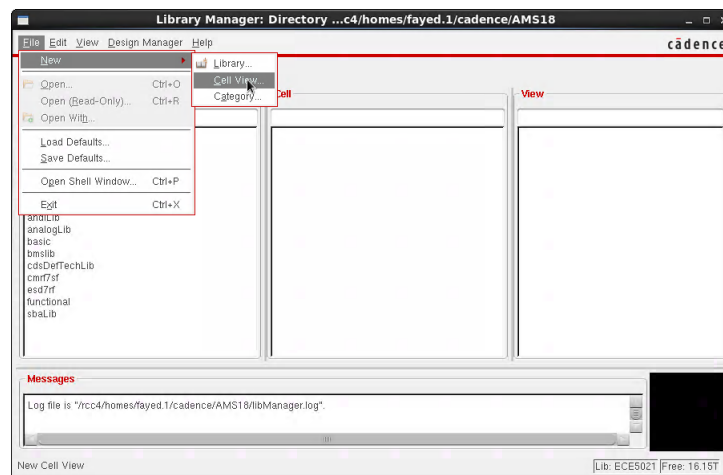
- A window with the results will appear as shown below



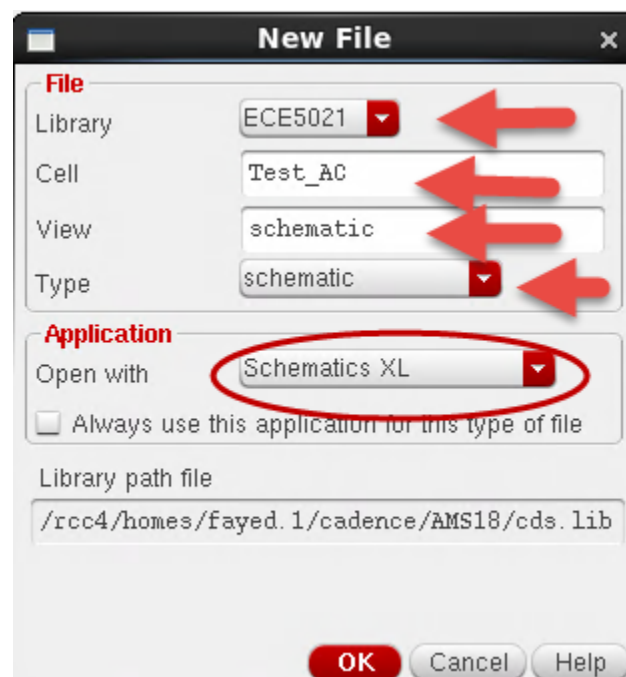
AC Simulations:

In this part, you will learn how to run AC simulations to plot the transfer function of a simple resistive-load common source amplifier using an NMOS transistor in the AMS 0.18 μm PDK.

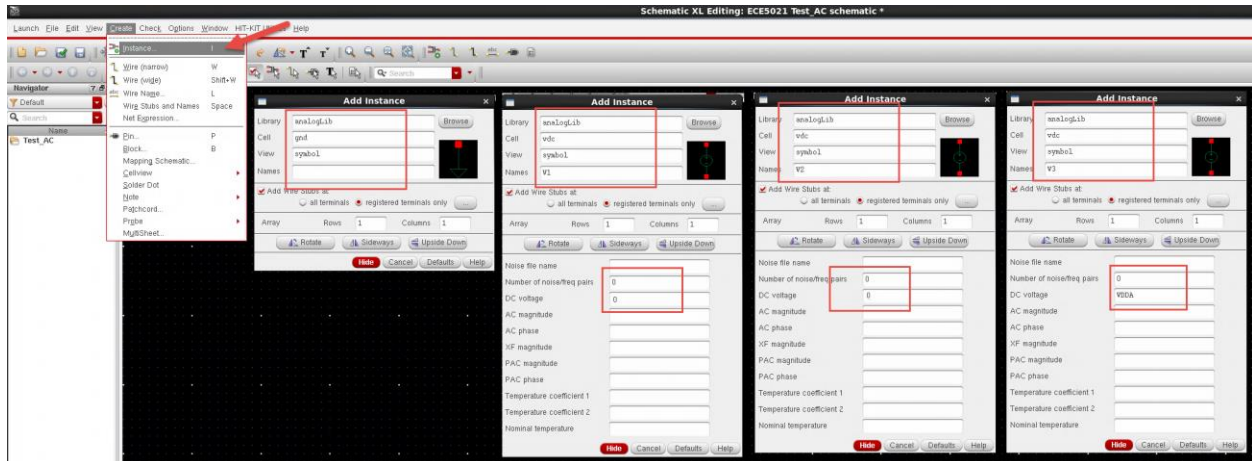
- Start Cadence by following step 3 of the PDK setup instructions (assuming you have gone through steps 1 and 2 at least once before)
- In the Library Manager, select the library you created in step 2 of the PDK setup instructions, or whatever library you created in the past and would like to use. Create a new cell view by going to “File >> New >> Cell View”



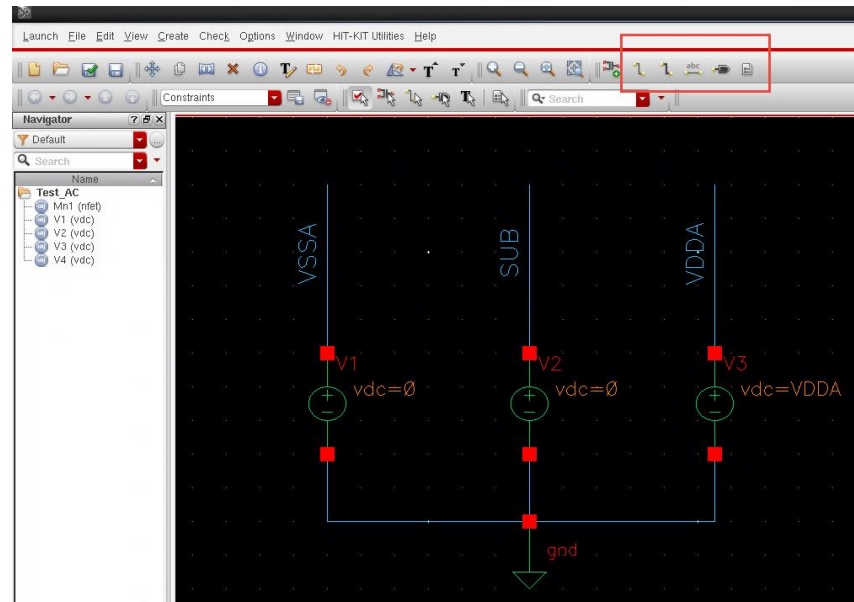
- The following window will appear. Fill in the fields as shown and click ok



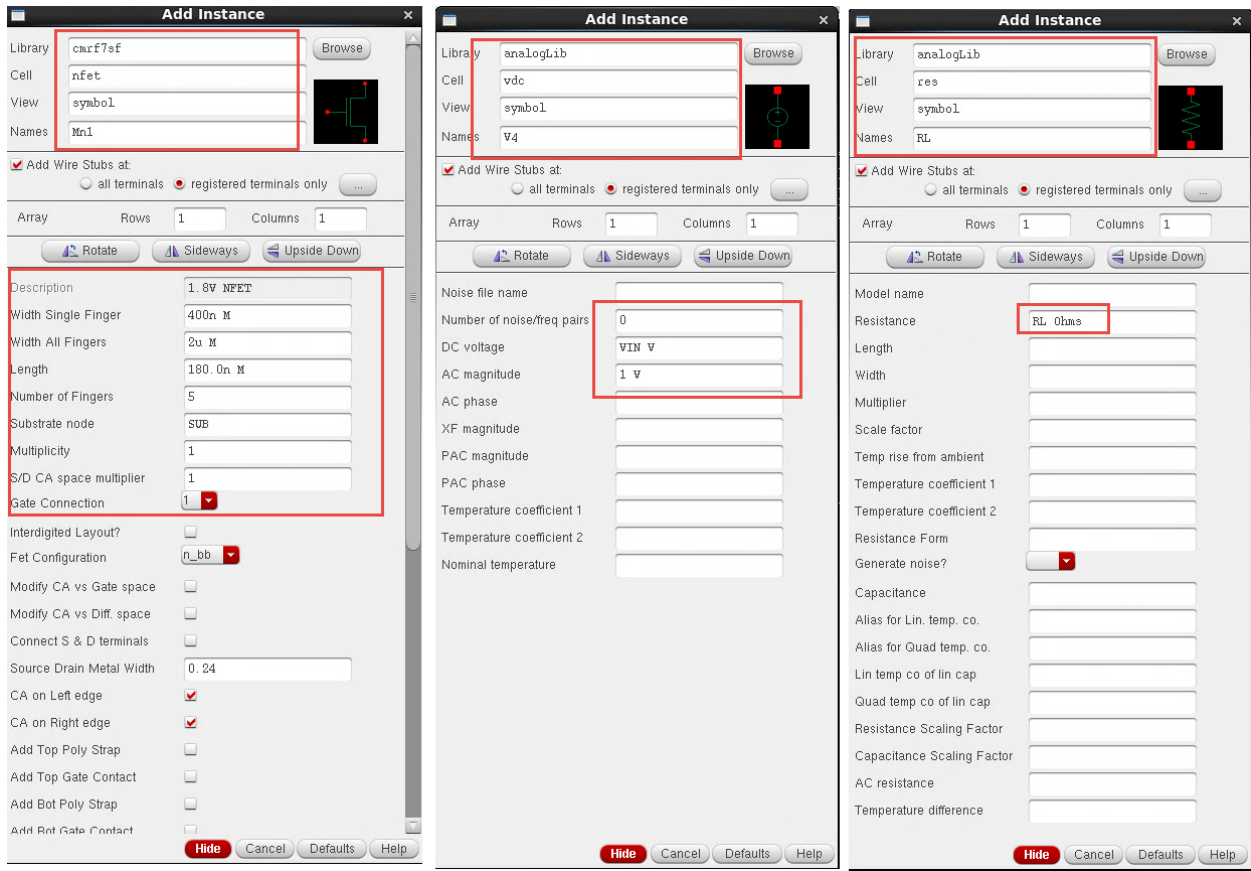
- A blank schematic window will appear as shown below. Use the “Create>>Instance” menu to instantiate a new component. You can also simply use the shortcut “i”. An add instance window will appear. Browse for each component shown below (one by one), and enter its parameters as shown below and click hide.



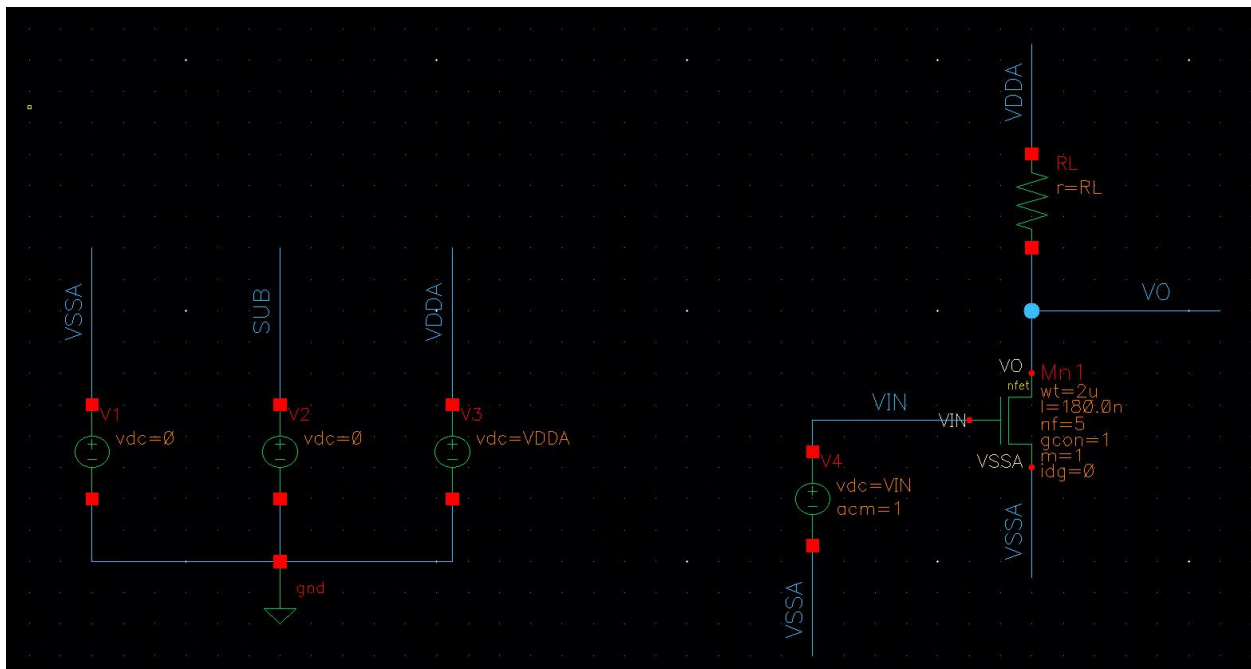
- Using the shortcuts at the top of the schematic window, connect the voltage sources and ground and name the wires as shown below



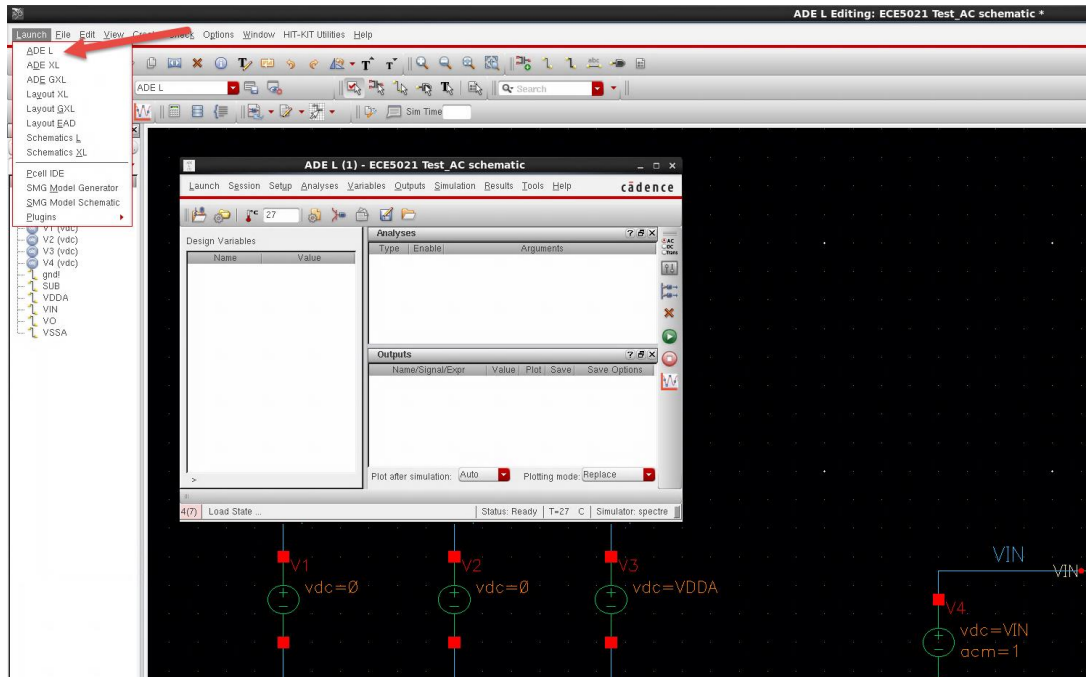
- Use the “Create>>Instance” menu to instantiate an NMOS transistor. Browse of the NMOS transistor in the PDK and enter its parameters as shown below. Also, instantiate a voltage source for the input voltage VIN and a resistor for the load resistor RL as shown below.



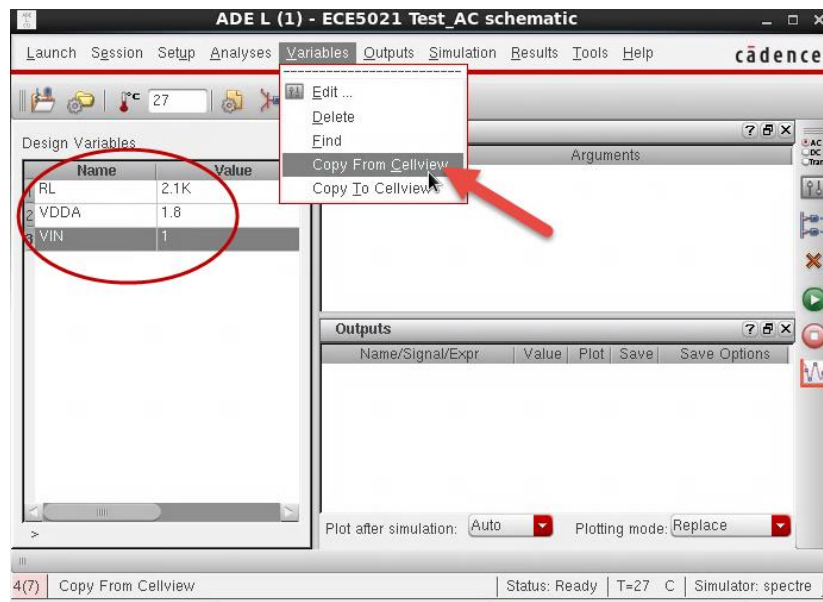
➤ Connect all the components as shown below



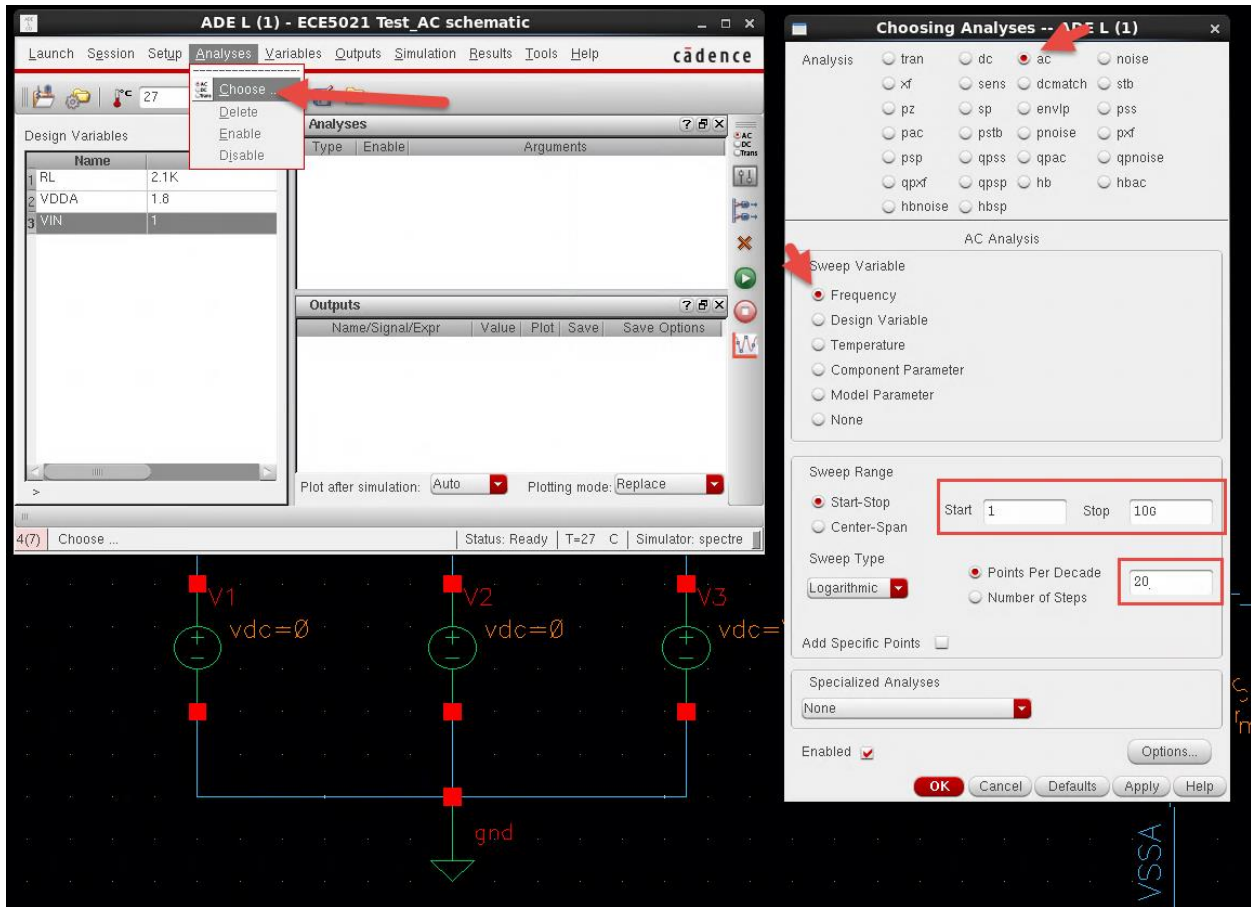
- Start the Analog Design Environment (ADE L) as shown below



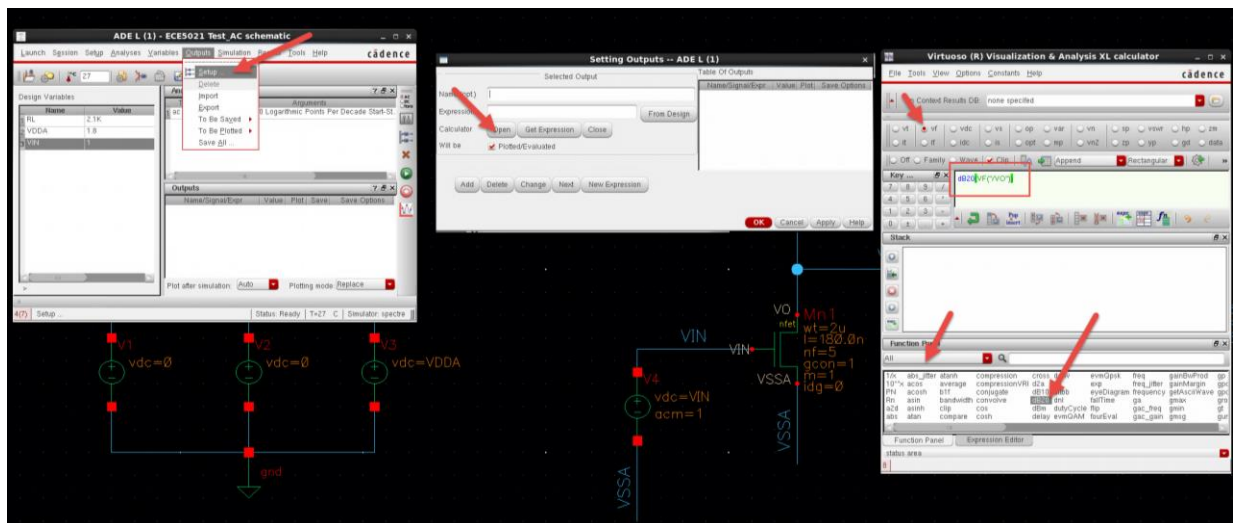
- To set VDD, VIN, and RL use the menu “Variables>>Copy from Cell View” to bring in these parameters from the schematic to ADE L. They will appear under Design Variables. You can set them to any value you like by double clicking each parameter. For this experiment, please set them as shown below.



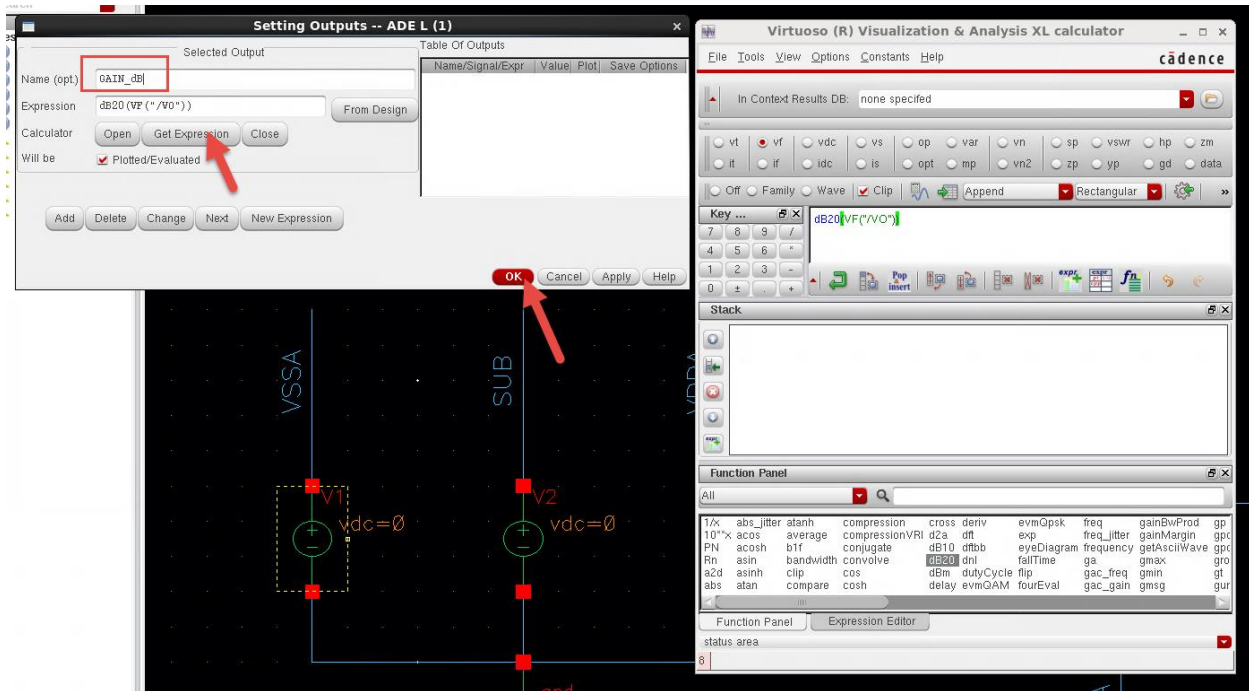
- Set up the AC analysis as shown below and click ok



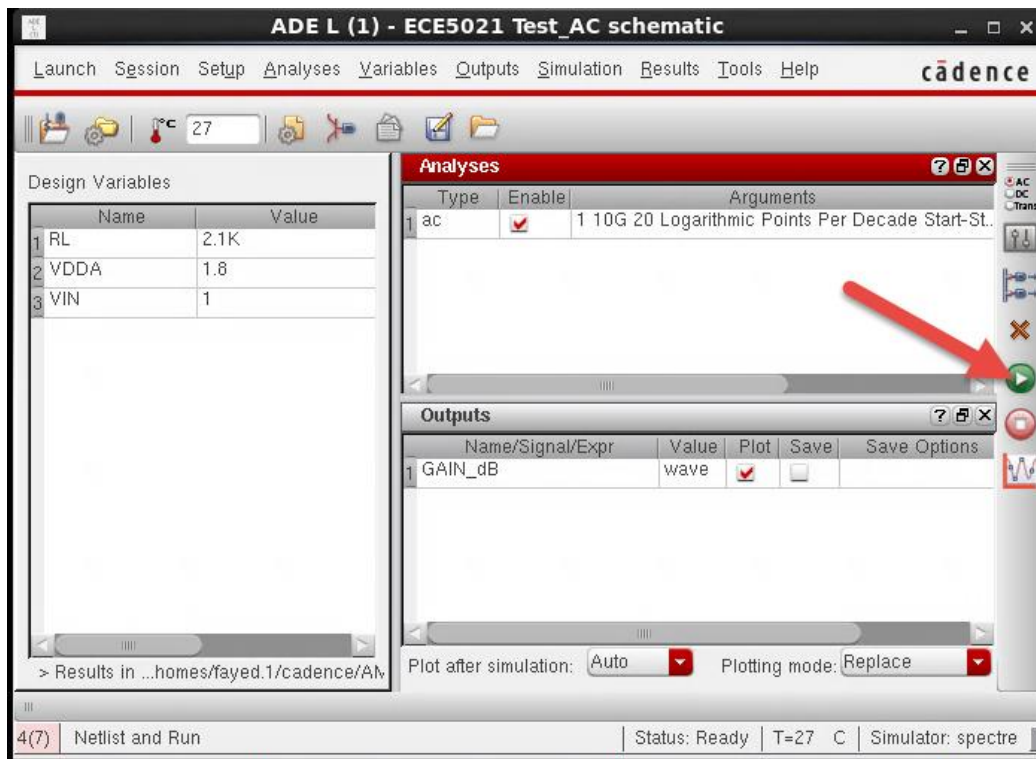
- To plot the transfer function between VO and VIN in dBs, you need to use the Calculator function as shown below.



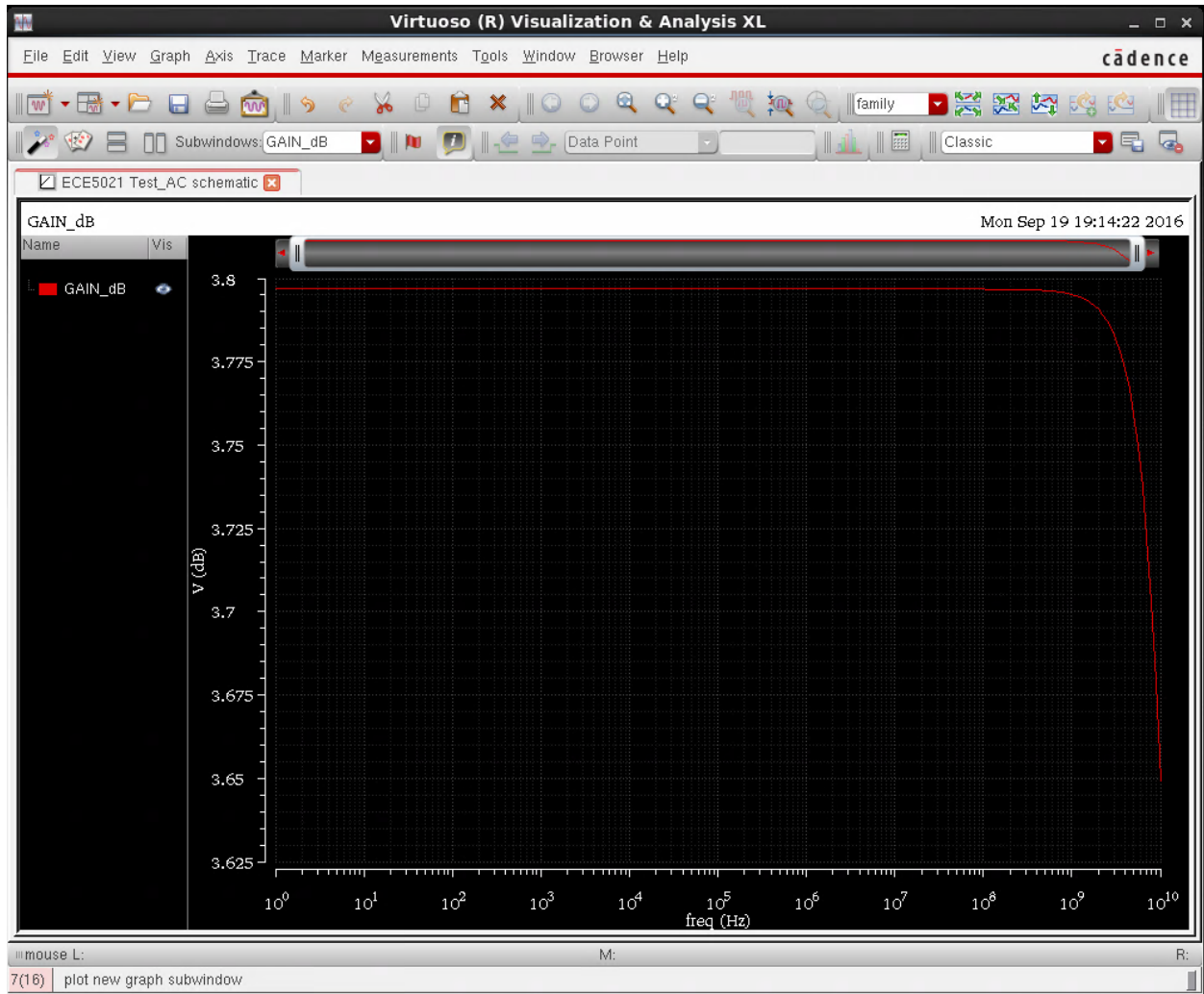
- To bring the expression back from the calculator into ADE, please do as shown below



- Start the simulation by clicking the play button



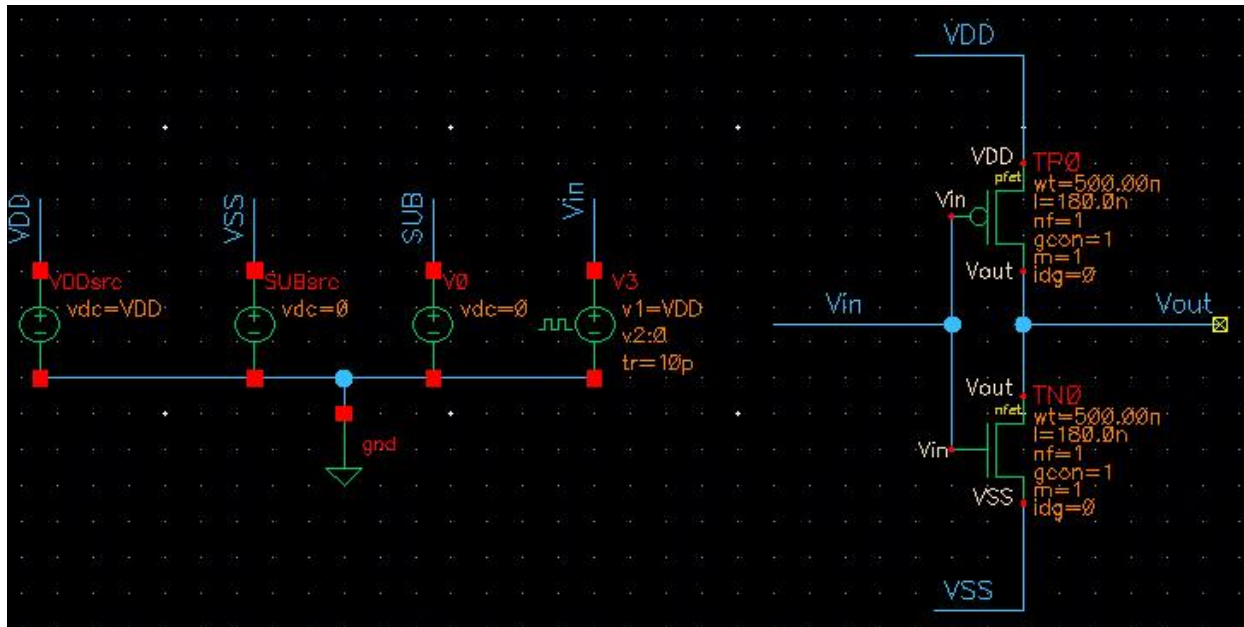
➤ A window with the results will appear as shown below



Transient Simulations:

In this part, you will learn how to run transient simulations to plot the waveform of an inverter using NMOS and PMOS transistors in the AMS 0.18 μm PDK.

- Make a new cell view as in “DC Simulations” and name it “Test_Transient.” Build the following inverter circuit, using “DC Simulation” as a reference. The voltage source for “Vin” is “vpulse” from “analogLib”, and the PMOS device is “pfet” from the “cmrf7sf” library.



- Notes:

- To edit the properties of a part, select that part and hit “Q”.
 - You can hit the “W” key to create a wire.
 - You can hit “L” to type in a node label, then click on the wire to which you would like to attach the label.
- For the voltage source of “Vin”, enter the parameters shown on the next page:

Edit Object Properties

Apply To: only current instance

Show: system user CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	analogLibs	off
Cell Name	vpulse	off
View Name	symbol	off
Instance Name	v3	off

Add Delete Modify

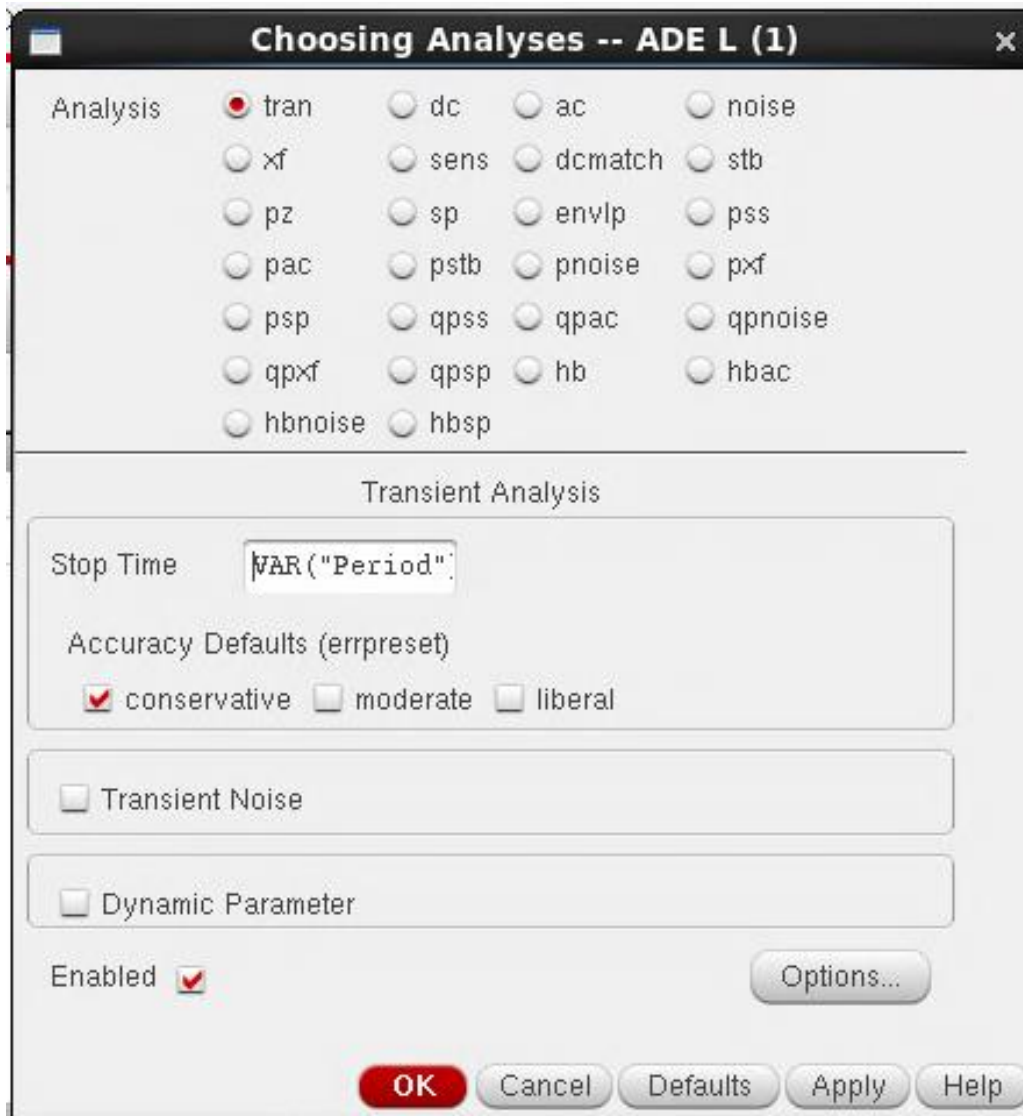
User Property	Master Value	Local Value	Display
Ivsignore	TRUE		off

CDF Parameter	Value	Display
Frequency name for 1/period		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage		off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	VDD V	off
Voltage 2	0 V	off
Period	Period s	off
Delay time	0 s	off
Rise time	10p s	off
Fall time	10p s	off
Pulse width	Period/2 s	off
Temperature coefficient 1		off

OK Cancel Apply Defaults Previous Next Help

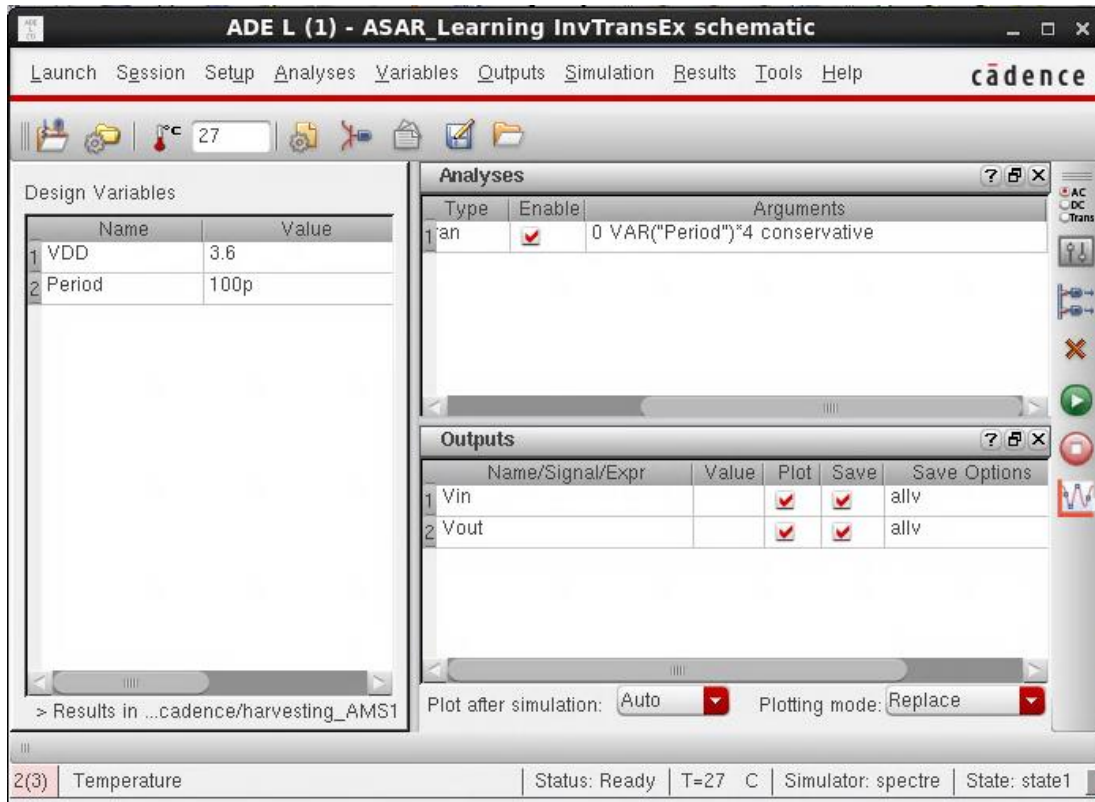
Last updated 08/11/2017

- In the properties for the pfet, keep the default lengths and widths, but change the “NWell node” to “VDD.” In the properties for the nfet, change the “Substrate node” to “SUB”.
- Select the check-and-save icon (the disk with the check mark over it) and start ADE L. Again, select “Analyses” and select “Choose” from the dropdown menu. This time, you will enter the following parameters:



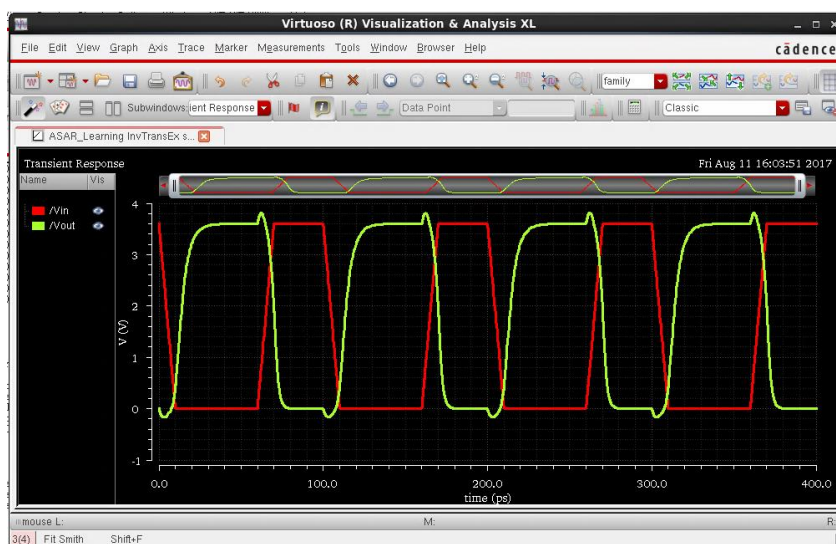
- Note that the entire stop time is not shown. For this, type in `VAR("Period")*4`.

- Set up the rest of your ADE L window to look like the image below. Once again, copy the variables from the cell view, and select “Vin” and “Vout” as outputs to be plotted.



- Hit the green play button on the right side of the ADE window to run the simulation. Note that simulations will not run if you have altered the circuit without clicking the “check and save” button.

Your results should look like this:

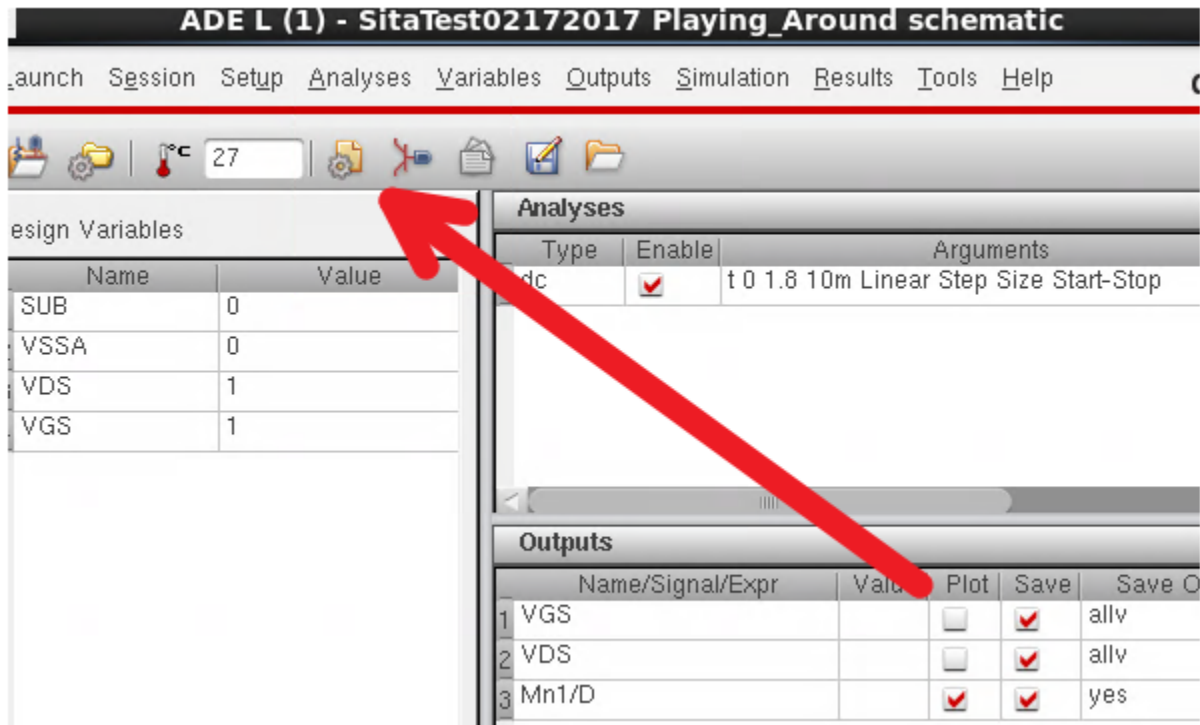


Last updated 08/11/2017

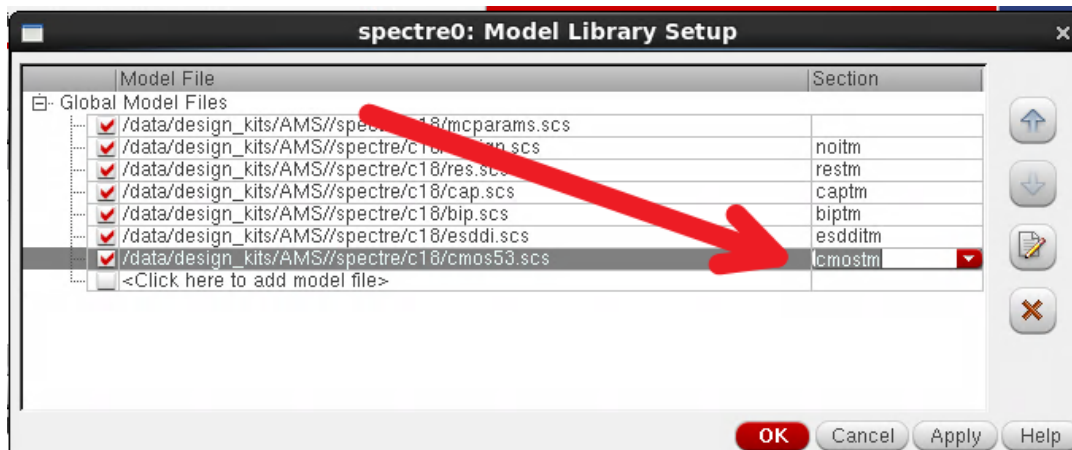
Changing Process Corners in Cadence

In this part, you will learn how to change process corners for any AC, DC, or transient simulation.

- In “ADE L,” click on the icon indicated.



- The process corner can be changed in the window indicated. “cmostm” is the “typical” or “normal” process corner, and is the default. “cmosff” is the fastest process corner, and “cmossf” is the slowest process corner.



- In an AC or DC simulation, you can simulate all of the process corners by selecting “append” in “plotting mode” at the bottom of the ADE L window, then hitting the “play” button each time after you change the process corner. If you do not close the plot, then all past traces will be saved on it. You will get a plot with traces that are the same color, but you can change their color by right-clicking on the legend for each trace and selecting “color” from the menu. You should be able to recreate the result below from your DC simulation.

